

# TC2-TC11

TEST 2  
MD-11-DZTCB-D

EP-DZTCB-D-DL-B  
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FICHE 1 OF 1

JUN 1977  
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The microfiche card displays a grid of 100 frames of data, organized into 10 rows and 10 columns. Each frame contains a small table or data set, with some frames showing graphical plots or waveforms. The data is printed in a light blue color on a dark background. The frames contain various types of information, including numerical data, text, and graphical representations of signals or waveforms. The overall layout is a dense grid of small data points and plots.

B01

EOF1DZDQOCSEQ  
PDP10 411

00010000

770608

PDP10 411

HDR1DZTCBDSEQ

00010000

770608

IDENTIFICATION

PRODUCT CODE:       MAINDEC-11-DZTCB-D-D  
PRODUCT NAME:        TC2-TC11 TEST #2  
PRODUCT DATE:        JULY 1977  
MAINTAINER:          DIAGNOSTIC ENGINEERING

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## DZTCB-D TC11 DECTAPE PROGRAM

## 1.0 GENERAL PROGRAM INFORMATION

## 1.1 ABSTRACT

TC2 - TC11 TEST2 IS USED TO TEST THE TC11 DECTAPE CONTROL. TC2 USES THE MAINTENANCE BIT FEATURE OF THE TC11 CONTROL TO CHECK THE TC11 CONTROL WITHOUT DEPENDING ON DECTAPE TRANSPORT MOVEMENT. PRIOR TO ACTUAL USE OF THE MAINTENANCE BIT FEATURE, CORRECT OPERATION OF THE INTERRUPT CIRCUITS IS CHECKED, AND THE MAINTENANCE BIT ITSELF IS CHECKED.

## 2.1.2 SYSTEM REQUIREMENTS

## 1.21 HARDWARE REQUIREMENTS

- A) PDP-11 SYSTEM (12k CORE).
- B) ASR33/35 TELETYPE.
- C) TC11 DECTAPE CONTROL AND AT LEAST ONE TUS6 DUAL TRANSPORT.

THE TELETYPE AND TC11 CONTROL MUST HAVE THEIR STANDARD PERIPHERAL ADDRESSES, INTERRUPT LEVELS, AND INTERRUPT VECTOR ADDRESSES. REFER TO SECTION 7.2 IF YOUR SYSTEM DOES NOT HAVE STANDARD PERIPHERAL ADDRESSES.

## 1.11 SOFTWARE REQUIREMENTS

THIS PROGRAM IS ABLE TO RUN "STAND ALONE" OR UNDER CONTROL OF THE ACT11 MONITOR

## 1.3 RELATED DOCUMENTS AND STANDARDS

SEE THE ACT11/XXDP PROGRAMERS GUIDE FOR INFORMATION ON RUNNING UNDER ACT 11

## 1.4 SUGGESTED PREREQUISITES

IT IS RECOMMENDED THAT ALL MAINDECS THAT CHECK OUT THE BASIC CPU BE RUN BEFORE TC2.

## 1.5 FAILURE ASSUMPTIONS

THROUGHOUT THIS PROGRAM IT IS ASSUMED THAT THE BASIC CPU IS IN GOOD RUNNING ORDER. IF IT IS NOT THE INFORMATION GAINED BY RUNNING THIS PROGRAM IS LIKELY TO BE FALSE (OR NONEXISTANT IF THE PROGRAM WILL NOT RUN).

## 2.0 OPERATING INSTRUCTIONS

## 2.10 LOADING PROCEDURES

THIS PROGRAM'S OBJECT TAPE IS PUNCHED IN ABSOLUTE FORMAT. THE ABS LOADER IS USED TO LOAD THE PROGRAM UNDER STAND ALONE MODE. FOR INFORMATION ON PROGRAM LOADING UNDER CONTROL OF THE VARIOUS MONITOR SYSTEMS, REFER TO THE DOCUMENTS NAMES IN SECTION 1.3 ABOVE. UNDER STAND ALONE MODE, AFTER ASCERTAINING THAT THE ABS LOADER PROGRAM IS IN THE PDP-11, FOLLOW THESE STEPS TO LOAD TC2:

- A) PUT THE TC2 BINARY TAPE INTO THE PAPER TAPE READER
- B) SET THE PDP-11 CONSOLE SWITCHES TO 37750
- C) DEPRESS LOAD ADDRESS
- D) DEPRESS START (TAPE SHOULD READ IN)

## 4.0 STARTING PROCEDURE

- A) UNIT 0: REMOTE/WRITE LOCK/. ALL OTHER UNITS OFF.
- B) WALL SWITCH ON, WRTM SWITCH OFF.
- C) LOAD ADDRESS 000200.
- D) PRESS START.
- E) THE PROGRAM IDENTIFIES ITSELF, TYPES SETUP INSTRUCTIONS, SR OPTIONS MESSAGE, AND HALTS.
- F) MAKE SURE THAT THE SETUP (STEPS A AND B) HAS BEEN PROPERLY DONE AND SELECT DESIRED SR OPTIONS, IF ANY. NORMAL SR SETTING IS 000000.
- G) PRESS CONT. THE PROGRAM BEGINS EXECUTION.
- H) AT THE END OF EACH PASS THE PASS COUNT IS PRINTED
- I) REFER TO SECTION 6.2 IF ERROR PRINTOUTS OCCUR.

#### 2.4 EXECUTION TIME

EXECUTION TIME IS DEPENDENT ON WHICH MODEL OF PDP11 THE PROGRAM IS TO BE RUN ON. ANY TIMES GIVEN APPLY TO THE PDP-11 MODEL 40 UNLESS OTHERWISE STATED

- A) ONE NORMAL ERROR FREE PASS TAKES APPROXIMATELY 10 SECONDS
- B) ONE SINGLE ITERATION PASS (SR11=1) TAKES ABOUT 5 SECONDS.

#### \*\*\*\*\*NOTE\*\*\*\*\*

THE SINGLE ITERATION PASS IS A CONVENIENT WAY TO QUICKLY DETERMINE IF ANY SOLID PROBLEMS EXIST. FOR A THOROUGH TEST, THE NORMAL ITERATION PASS SHOULD BE RUN.

#### 6.0 ERROR INFORMATION

ERRORS ARE REPORTED IN THIS PROGRAM BY THE FOLLOWING METHODS:

- A) UNCONDITIONAL ERROR HALTS, OR
- B) ERROR PRINTOUT FOLLOWED BY OPTIONAL ERROR HALT.

#### 6.1 UNCONDITIONAL ERROR HALTS

AN UNCONDITIONAL ERROR HALT WILL OCCUR AT THE ADDRESSES LISTED BELOW IF THROUGH HARDWARE OR SOFTWARE FAILURE, PROGRAM CONTROL IS TRANSFERRED TO AN UNEXPECTED AREA BETWEEN 000000 AND 000176.

000002 RESERVED AREA  
 000016 DEBUG TRAP  
 000022 IOT TRAP

000040 THROUGH 000176 - SYSTEM SOFTWARE AND INTERRUPT VECTOR AREA  
 TO FIND OUT WHERE THE PROGRAM WAS AT THE TIME THE FAILURE OCCURRED,

- A) EXAMINE CONTENTS OF REGISTER 6. (ADDRESS 177706).
- B) TRANSFER THE CONTENTS OF REG 6 TO THE SR, LOAD ADDRESS AND EXAMINE.
- C) THE DATA SHOWN IN THE DATA LIGHTS IS THE VALUE OF THE PC WHEN THE FAILURE OCCURRED.
- D) LOCATE IN PROGRAM LISTING THE DISPLAYED PC VALUE.
- E) THE INSTRUCTION THAT IMMEDIATELY PRECEDES THE ONE REFERENCED BY THE DISPLAYED PC VALUE IS THE INSTRUCTION THAT WAS/WAS BEING EXECUTED WHEN THE FAILURE OCCURRED.

AN UNCONDITIONAL ERROR HALT FAILURE IS AN ABNORMAL CONDITION INDICATING A HARDWARE FAILURE, OR MOST UNLIKELY, A PROGRAM FAILURE. THIS PROGRAM ASSUMES THAT THE PROCESSOR IS IN OPERATING CONDITION IN ORDER TO PERFORM ITS TESTS. ANY FURTHER STEPS REQUIRED TO DIAGNOSE AN UNCONDITIONAL ERROR HALT ARE NOT WITHIN THE SCOPE OF THIS PROGRAM.

## 6.2 ERROR PRINTOUTS

THERE ARE 2 TYPES OF ERROR PRINTOUTS, NORMAL ERROR PRINTOUTS AND FATAL ERROR PRINTOUTS. EACH TYPE IS GENERATED BY THE SYSMAC .SERROR SUBROUTINE. THE ".SERROR" SUBROUTINE IS CALLED BY AN "ERROR NN(TRAP+N)" STATEMENT IN THE PROGRAM LISTING. A NORMAL ERROR PRINTOUT LOOKS AS FOLLOWS:

```
PC      SP      PS      TEST      TCCM      TCST      ADDITIONAL INFO
XXXXXX XXXXXX XXXXXX XXXXXX XXXXXX XXXXXX XXXXXX XXXXXX
```

WHERE:

PC  
XXXXXX IS THE ADDRESS OF THE ERROR CALL

SP  
XXXXXX IS THE VALUE OF THE STACK POINTER

PS  
XXXXXX IS THE VALUE OF THE PROCESSOR STATUS WORD

TEST  
XXXXXX IS THE NUMBER OF THE FAILING ROUTINE

TCCM  
XXXXXX IS THE VALUE OF THE DECTAPE COMMAND REGISTER

TCST  
XXXXXX IS THE CONTENTS OF THE DECTAPE STATUS REGISTER

ADDITIONAL INFORMATION CAN VARY FROM TEST TO TEST AND FURTHER DESCRIBES THE ERROR. AFTER THE PRINTOUT IS COMPLETED, THE PROGRAM WILL HALT AT COMMON ERROR HALT IF SR15 IS SET. WHEN AN ERROR PRINTOUT OCCURS:

- A) LOOK UP THE ADDRESS REFERENCED BY PC OYYYYY IN THE LISTING.
- B) OPPOSITE THE PC VALUE AN "ERROR" STATEMENT WILL BE FOUND, AND IN THE COMMENTS SECTION, A DESCRIPTION OF THE ERROR.
- C) AT THE BEGINNING OF THE TEST ROUTINE A DESCRIPTION OF THE TEST WILL BE FOUND.

FATAL ERRORS ARE UNEXPECTED TRAPS TO EITHER LOCATION 4 OR TO LOCATION 10. WHEN THESE OCCUR A FATAL ERROR MESSAGE IS PRINTED OUT IN THE FOLLOWING FORMAT.

FATAL ERROR TRAP TO LOC XX FROM LOCATION XXXXXX

WHERE X IS THE TRAP VECTOR LOCATION(4 OR 10) AND XXXXXX IS THE PLACE THAT THE PROGRAM WAS EXECUTING AT WHEN THE FATAL ERROR TRAP OCCURRED. AFTER THE MESSAGE IS PRINTED THE PROGRAM ATTEMPTS TO RESTART ITSELF AT LOCATION 000200 THE STANDARD SR OPTIONS ARE DESCRIBED HERE.

SR15 HALT ON ERROR. WITH SR15 SET TO A 1, THE PROGRAM WILL HALT AFTER AN ERROR OCCURS. PRESSING 'CONT WILL CAUSE PROGRAM TO RESUME OPERATION.

SR14 SCOPE. THIS OPTION CAUSES THE PROGRAM TO REMAIN IN THE CURRENT TEST ROUTINE. WHEN THE OPTION IS REMOVED, THE PROGRAM WILL COMPLETE THE CURRENT ROUTINE, AND WILL THEN GO ON TO THE NEXT ROUTINE.

SR13 INHIBIT ERROR PRINTOUT. THIS OPTION IF SET, WILL REMOVE ALL ERROR PRINTOUTS.

SR11 PROGRAM TO EXECUTE EACH TEST ONLY ONCE, INSTEAD OF THE NORMAL NUMBER OF ITERATIONS SELECTED FOR EACH TEST. THIS ALLOWS FOR A "QUICK CHECK" OF THE TC11 HARDWARE.

SR10 BELL ON ERROR. SETTING THIS SWITCH TO A 1 WILL CAUSE THE PROGRAM TO SOUND THE BELL WHEN AN ERROR IS FOUND. THIS SWITCH DOES NOT INTERFERE WITH THE FUNCTIONS OF SW15 AND SW13

SR08 SELECT ROUTINE. WITH SR8 SET, THE PROGRAM WILL RUN NORMALLY UNTIL THE ROUTINE SPECIFIED IN SR7 THROUGH SR0 IS ENCOUNTERED. THE PROGRAM WILL REMAIN LOOPING IN THE SPECIFIED ROUTINE, UNTIL EITHER SR8 IS CHANGED, OR UNTIL THE VALUE OF SWITCHES SR7 THROUGH SR0 CHANGES

SR7-SR0 TEST SELLECT. THE NUMBER SET IN THESE SWITCHES IS THE NUMBER OF THE TEST THAT WILL BE LOCKED ONTO IF SR8 IS SET IF SR8 IS SET TO A 0 THEN SR7 THROUGH SR0 HAVE NO EFFECT ON THE OPERATION OF THE PROGRAM

## 7.2 TESTING TC11 AT NON-STANDARD ADDRESSES AND/OR VECTORS

THIS PROGRAM CAN TEST THE TC11 AT NON-STANDARD ADDRESSES AND VECTORS PROVIDED THOSE ADDRESSES AND VECTORS ARE PROVIDED TO THE PROGRAM AS FOLLOWS:

A) AFTER LOADING PROGRAM REFER TO PROGRAM LISTING AND CHANGE LOCATIONS 001004 THROUGH 001020 TO REFLECT THE NEW TC11 ADDRESSES AND VECTORS.

B) PROCEED TO USE THE PROGRAM, OR

## 7.0 PROGRAM LISTING

31		OPERATIONAL SWITCH SETTINGS
55		BASIC DEFINITIONS
168		TRAP CATCHER
178		STARTING ADDRESS(ES)
342		COMMON TAGS
478		ERROR POINTER TABLE
870		INITIALIZE THE COMMON TAGS
924	T0001	
938	T0002	
953	T0003	
967	T0004	
983	T0005	
1004	T0006	
1021	T0007	
1039	T0010	
1060	T0011	
1082	T0012	
1109	T0013	
1134	T0014	
1150	T0015	
1169	T0016	
1200	T0017	
1230	T0020	
1251	T0021	
1280	T0022	
1301	T0023	
1331	T0024	
1356	T0025	
1384	T0026	
1411	T0027	
1439	T0030	
1464	T0031	
1518	T0032	
1578	T0033	
1624	T0034	
1672	T0035	
1720	T0036	
1767	T0037	
1804	T0040	
1870	T0041	
1939	T0042	
1987	T0043	
2041	T0044	
2081	T0045	
2141	T0046	
2153	T0047	
2164	T0050	
2175	T0051	
2186	T0052	
2197	T0053	
2211	T0054	
2222	T0055	
2265	T0056	
2268		END OF PASS ROUTINE
2607		SCOPE HANDLER ROUTINE
2691		ERROR HANDLER ROUTINE

H01

MAINDEC-11-DZTCB-D TC11 TEST #2 MACY11 27(1006) 18-FEB-77 11:33  
DZTCB0.P11 18-FEB-77 10:59 TABLE OF CONTENTS

2751 POWER DOWN AND UP ROUTINES  
2820 TYPE ROUTINE  
2892 CONVERT BINARY TO DECIMAL AND TYPE ROUTINE  
2968 BINARY TO OCTAL (ASCII) AND TYPE  
3047 ERROR MESSAGE TYPEOUT ROUTINE  
3097 TRAP DECODER  
3149 TRAP TABLE



1  
2  
3  
4  
5  
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56  
57  
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59  
60

167400  
000000

000000

000000

000000

000000

```

.ABS
.ENABL AMA
.LIST MC,MD,BIN,LD,SEQ,ME
.NLIST CND
$SWR=167400
$TN=0
.ENABL ABS
.MCALL .HEADER,.SCATCH,.SEOP,.EQUAT
.MCALL .SWRHI,.SWRLO,$SCOPE,SETUP
.MCALL .STYPOCT,.STYPDEC,.STRAP,$POWER
.MCALL .SERRROR,.STYPE,STARS,.SERRTYP
.MCALL .SCTAG
.SETUP (. $SCOPE,.SEOP,$POWER,.STRAP,.SERRROR)
.LIST
.HEADER (MAINDEC-11-DZTCB-D TC11 TEST #2), (1972,1977), (J. COMEAU)
.TITLE MAINDEC-11-DZTCB-D TC11 TEST #2
.#COPYRIGHT (C) 1972,1977
.#DIGITAL EQUIPMENT CORP.
.#MAYNARD, MASS. 01754
.#
.#PROGRAM BY J. COMEAU
.#
.#THIS PROGRAM WAS ASSEMBLED USING THE PDP-11 MAINDEC SYSMAC
.#PACKAGE (MAINDEC-11-DZQAC-C3), JAN 19, 1977.
.#
.SWRHI
.SBTTL OPERATIONAL SWITCH SETTINGS
.*
.* SWITCH USE
.* -----
.* 15 HALT ON ERROR
.* 14 LOOP ON TEST
.* 13 INHIBIT ERROR TYPEOUTS
.* 11 INHIBIT ITERATIONS
.* 10 BELL ON ERROR
.* 9 LOOP ON ERROR
.LIST
.* 8 LOOP ON TEST IN SWR<7:0>
.MACRO .SWRLO S07,S06,S05,S04,S03,S02,S01,S00
.IIF NB <S07>,* 7 S07
.IIF NB <S06>,* 6 S06
.IIF NB <S05>,* 5 S05
.IIF NB <S04>,* 4 S04
.IIF NB <S03>,* 3 S03
.IIF NB <S02>,* 2 S02
.IIF NB <S01>,* 1 S01
.IIF NB <S00>,* 0 S00
.ENDM
.* SWRLO
.* 7-0 # OF TEST TO LOOP ON IF SWR<8> IS SET
.EQUAT
.SBTTL BASIC DEFINITIONS
.*INITIAL ADDRESS OF THE STACK POINTER *** 1100 ***

```

57 001100  
58  
59  
60  
61  
62 000011  
63 000012  
64 000015  
65 000200  
66 177776  
67  
68 177774  
69 177772  
70 177570  
71 177570  
72  
73  
74 000000  
75 000001  
76 000002  
77 000003  
78 000004  
79 000005  
80 000006  
81 000007  
82 000006  
83 000007  
84  
85  
86 000000  
87 000040  
88 000100  
89 000140  
90 000200  
91 000240  
92 000300  
93 000340  
94  
95  
96 100000  
97 040000  
98 020000  
99 010000  
100 004000  
101 002000  
102 001000  
103 000400  
104 000200  
105 000100  
106 000040  
107 000020  
108 000010  
109 000004  
110 000002  
111 000001  
112

STACK= 1100  
.EQUIV FMT,ERROR ;: BASIC DEFINITION OF ERROR CALL  
.EQUIV TOT,SCOPE ;: BASIC DEFINITION OF SCOPE CALL  
;#MISCELLANEOUS DEFINITIONS  
HT= 11 ;: CODE FOR HORIZONTAL TAB  
LF= 12 ;: CODE FOR LINE FEED  
CR= 15 ;: CODE FOR CARRIAGE RETURN  
CRLF= 200 ;: CODE FOR CARRIAGE RETURN-LINE FEED  
PS= 177776 ;: PROCESSOR STATUS WORD  
.EQUIV PS,PSW  
\$TKLMT= 177774 ;: STACK LIMIT REGISTER  
PIRQ= 177772 ;: PROGRAM INTERRUPT REQUEST REGISTER  
DSWR= 177570 ;: HARDWARE SWITCH REGISTER  
DDISP= 177570 ;: HARDWARE DISPLAY REGISTER  
;#GENERAL PURPOSE REGISTER DEFINITIONS  
R0= %0 ;: GENERAL REGISTER  
R1= %1 ;: GENERAL REGISTER  
R2= %2 ;: GENERAL REGISTER  
R3= %3 ;: GENERAL REGISTER  
R4= %4 ;: GENERAL REGISTER  
R5= %5 ;: GENERAL REGISTER  
R6= %6 ;: GENERAL REGISTER  
R7= %7 ;: GENERAL REGISTER  
SP= %6 ;: STACK POINTER  
PC= %7 ;: PROGRAM COUNTER  
;#PRIORITY LEVEL DEFINITIONS  
PR0= 0 ;: PRIORITY LEVEL 0  
PR1= 40 ;: PRIORITY LEVEL 1  
PR2= 100 ;: PRIORITY LEVEL 2  
PR3= 140 ;: PRIORITY LEVEL 3  
PR4= 200 ;: PRIORITY LEVEL 4  
PR5= 240 ;: PRIORITY LEVEL 5  
PR6= 300 ;: PRIORITY LEVEL 6  
PR7= 340 ;: PRIORITY LEVEL 7  
;#"SWITCH REGISTER" SWITCH DEFINITIONS  
SW15= 100000  
SW14= 40000  
SW13= 20000  
SW12= 10000  
SW11= 4000  
SW10= 2000  
SW09= 1000  
SW08= 400  
SW07= 200  
SW06= 100  
SW05= 40  
SW04= 20  
SW03= 10  
SW02= 4  
SW01= 2  
SW00= 1  
.EQUIV SW09,SW9



```

169      000000
170
171
172
173
174      000174
175 000174 000000
176 000176 000000
177
178 000200 000137 002312
179
180      001000
181      000240
182      000000
183      100000
184      005746
185      024646
186      005726
187      022626
188      000007
189      177777
190      000003
191      000207
192      000040
193      177777
194      106000
195      040000
196      020000
197      000000
198      000004
199      000010
200      000014
201      000020
202      000024
203      000030
204      000034
205      020000
206      010000
207      004000
208      000000
209 000204 000240
210      000000
211      000400
212      001000
213      001400
214      002000
215      002400
216      003000
217      003400
218      000100
219      000000
220      000002
221      000004
222      000006
223      000010
224      000012

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```

      .=0
;#ALL UNUSED LOCATIONS FROM 4 - 776 CONTAIN A ".+2,HALT"
;#SEQUENCE TO CATCH ILLEGAL TRAPS AND INTERRUPTS
;#LOCATION 0 CONTAINS 0 TO CATCH IMPROPERLY LOADED VECTORS
.LIST
      .=174
DISPREG: .WORD 0           ;; SOFTWARE DISPLAY REGISTER
SWREG:   .WORD 0           ;; SOFTWARE SWITCH REGISTER
.SBTTL   STARTING ADDRESS(ES)
JMP      @#START ;; JUMP TO STARTING ADDRESS OF PROGRAM
;EQUATES
SPBOT=1000
NOP=240
OPEN=0
MANUAL=BIT15
PUSH=005746
PUSH2=024646
POPSP=005726
POPSP2=022626
BELL=007
TLAST=-1
TRC=3
RTSPC=207
I=40
X=-1
A=BIT15
B=BIT14
C=BIT13
V0=0
V1=4
V2=10
V3=14
V4=20
V5=24
V6=30
V7=34
MAINT=BIT13
DINH=BIT12
REV=BIT11
FWD=0
NOP
U0=0
U1=BIT8
U2=BIT9
U3=BIT9!BIT8
U4=BIT10
U5=BIT10!BIT8
U6=BIT10!BIT9
U7=BIT10!BIT9!BIT8
IE=BIT6
SAT=0
RNUM=BIT1
ROATA=BIT2
RALL=BIT2!BIT1
SST=BIT3
WRTM=BIT3!BIT1

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277  
278  
279  
280

000014  
000016  
000001  
000000

```

WDATA=BIT3!BIT2
WALL=BIT3!BIT2!BIT1
DO=BIT0
EMTX=0
.MACRO ADITAG
TCST: 177340
ICCM: 177342
TCWC: 177344
TCBA: 177346
ICDT: 177350
TCVTR: 214
TCLVL: 300
TPS: 177564
TPB: 177566
COOCAL: OPEN
RTNNO: OPEN
NXTST: OPEN
CURTST: OPEN
CRBUF: OPEN
CRBUFA: OPEN
CTRA: OPEN
SBOAT1: 50505
          127272
SBOAT2: 72727
SBOAT3: 105050
          72727
          105056
POWPUS: .WORD 000000
POWPOP: .WORD 000000
TCMT: OPEN
TCSTT: OPEN
.ENDM ADITAG

```

```

;TC11 STATUS REGISTER.
;TC11 COMMAND REGISTER.
;TC11 WORD COUNT REGISTER.
;TC11 BUS ADDRESS REGISTER.
;TC11 DATA REGISTER.
;TC11 INTERRUPT VECTOR
;TC11 INTERRUPT PRIORITY LEVEL.
;LSP CSR
;LSP BUFFER

```

```

.MACRO SETRAP
MOV #TRAP0,2#4 ;SETUP FATAL TRAP VECTOR JUST IN CASE
MOV #340,2#6 ;NO INTERRUPTS WHILE SERVICING FATAL ERRORS
.ENDM SETRAP
.MACR C55 ;MTK CODE 55. REV END ZONE MARK.
.BYTE I,0,I,I,0,I
.ENDM
.MACR C25 ;MTK CODE 25. EXTENSION MARK.
.BYTE 0,I,0,I,0,I
.ENDM
.MACR C26 80,81,82,83,84,85 ;FWD BLOCK MARK.
.BYTE 0!80,I!81,0!82,I!83,I!84,0!85
.ENDM
.MACR C32 80,81,82,83,84,85 ;REV GUARD.
.BYTE 0!80,I!81,I!82,0!83,I!84,0!85
.ENDM
.MACR C10 80,81,82,83,84,85 ;MTK CODE 10.
.BYTE 0!80,0!81,I!82,0!83,0!84,0!85
.ENDM
.MACR C70 80,81,82,83,84,85 ;MTK CODE 70. DATA MARK.
.BYTE I!80,I!81,I!82,0!83,0!84,0!85
.ENDM

```

NO1

MAINDEC-11-DZTCB-D TC11 TEST #2  
DZTCB0.P11 18-FEB-77 10:59

MACY11 27(1006) 18-FEB-77 11:33 PAGE 6  
STARTING ADDRESS(ES)

281  
282  
283  
284  
285  
286  
287  
288  
289  
290  
291  
292  
293  
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```

.MACR C73      80,81,82,83,84,85
.BYTE  I!80,I!81,I!82,0!83,I!84,I!85 ;MTK CODE 73. DATA MARK.
.ENDM
.MACR C51      80,81,82,83,84,85
.BYTE  I!80,0!81,I!82,0!83,0!84,I!85 ;MTK CODE 51. FWD GUARD.
.ENDM
.MACR C45      80,81,82,83,84,85
.BYTE  I!80,0!81,0!82,I!83,0!84,I!85 ;MTK CODE 45. REV BLOCK MARK.
.ENDM
.MACR C22
.BYTE  0,I,0,0,I,0 ;MTK CODE 22. FWD END ZONE.
.ENDM
.MACR CEND
.BYTE  -1
.ENDM
.MACR EMT
.BYTE  I,I,I,0,0,I
.ENDM
.MACR MTCOD MTADR,CNT
JSR    RS,LMTCOD ;CALL LOAD MT CODES SUB.
MTADR  ;ADDRESS OF MARK TRACK CODES.
CNT    ;MARK TRACK CODE COUNT.
.ENDM
.MACR MTCOE CALADR,MTADR,CNT
JSR    RS,LMTCOE ;CALL LOAD MT CODES SUBROUTINE.
CALADR ;ADDR TO GO AFTER EACH CODE PASSED.
MTADR  ;ADDRESS OF MARK TRACK CODES.
CNT    ;MARK TRACK CODE COUNT.
.ENDM
.MACR EMTDEF NAMEA,NAMEB
.WORD  NAMEB ;POINTER FOR EMT CALL NAMEA
.NLIST
NAMEA=EMT+EMTX
EMTX=EMTX+1
.LIST
.ENDM
.MACRO SCOMAC
CLR    @TCCM
CLR    2(SP) ;PS TO =0 AFTER WE EXIT THE SCOPE ROUTINE
JSR    PC,SRSETT
JSR    PC,RSTMTK
.ENDM
.=50
.WORD  0
.WORD  0
.SCHTAG 10,10,ADITAG,1100
.MACRO $$SCHREG A,B
SREG'A: .WORD 0 ;;CONTAINS (($REGAD)+'B)
.NLIST
SCH1=$SCH1+1
SCH2=$SCH2+2
.LIST
.ENDM $$SCHREG
.MACRO $$SCHTMP A
STMP'A: .WORD 0 ;;USER DEFINED
.NLIST

```

000050 000050  
000052 000000  
000054 000000

B02

MAINDEC-11-DZTCB-D TC11 TEST #2  
DZTCB0.P11 18-FEB-77 10:59

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STARTING ADDRESS(ES)

337  
338  
339  
340

SCM4=SCM4+1  
.LIST  
.ENDM SSCMTMP  
.PAGE





```

397 .LIST
398 001172 S$CHREG \SCM1,\SCM2
399 001172 000000 $REG4: .WORD 0 ;;CONTAINS (($REGAD)+10)
400 .LIST
401 001174 S$CHREG \SCM1,\SCM2
402 001174 000000 $REG5: .WORD 0 ;;CONTAINS (($REGAD)+12)
403 .LIST
404 001176 S$CHREG \SCM1,\SCM2
405 001176 000000 $REG6: .WORD 0 ;;CONTAINS (($REGAD)+14)
406 .LIST
407 001200 S$CHREG \SCM1,\SCM2
408 001200 000000 $REG7: .WORD 0 ;;CONTAINS (($REGAD)+16)
409 .LIST
410 .LIST
411 000010 .REPT 10
412 S$CHTMP \SCM4
413 .ENDR
414 001202 S$CHTMP \SCM4
415 001202 000000 $TMP0: .WORD 0 ;;USER DEFINED
416 .LIST
417 001204 S$CHTMP \SCM4
418 001204 000000 $TMP1: .WORD 0 ;;USER DEFINED
419 .LIST
420 001206 S$CHTMP \SCM4
421 001206 000000 $TMP2: .WORD 0 ;;USER DEFINED
422 .LIST
423 001210 S$CHTMP \SCM4
424 001210 000000 $TMP3: .WORD 0 ;;USER DEFINED
425 .LIST
426 001212 S$CHTMP \SCM4
427 001212 000000 $TMP4: .WORD 0 ;;USER DEFINED
428 .LIST
429 001214 S$CHTMP \SCM4
430 001214 000000 $TMP5: .WORD 0 ;;USER DEFINED
431 .LIST
432 001216 S$CHTMP \SCM4
433 001216 000000 $TMP6: .WORD 0 ;;USER DEFINED
434 .LIST
435 001220 S$CHTMP \SCM4
436 001220 000000 $TMP7: .WORD 0 ;;USER DEFINED
437 .LIST
438 001222 000000 $TIMES: 0 ;;MAX. NUMBER OF ITERATIONS
439 001224 000000 $ESCAPE: 0 ;;ESCAPE ON ERROR ADDRESS
440 001226 177607 000377 $BELL: .ASCIZ <207><377><377> ;;CODE FOR BELL
441 001232 077 $QUES: .ASCII /?/ ;;QUESTION MARK
442 001233 015 $CRLF: .ASCII <15> ;;CARRIAGE RETURN
443 001234 000012 $LF: .ASCIZ <12> ;;LINE FEED
444 001236 STARS
445 *****
446 .IRP A,<ADITAG>
447 A
448 .ENDM
449 001236 ADITAG
450 001236 177340 TCST: 177340 ;;TC11 STATUS REGISTER.
451 001240 177342 ICCM: 177342 ;;TC11 COMMAND REGISTER.
452 001242 177344 TCWC: 177344 ;;TC11 WORD COUNT REGISTER,

```

:TC11 BUS ADDRESS REGISTER.  
:TC11 DATA REGISTER.  
:TC11 INTERRUPT VECTOR  
:TC11 INTERRUPT PRIORITY LEVEL.  
:LSP CSR  
:LSP BUFFER

453 001244 177346  
454 001246 177350  
455 001250 000214  
456 001252 000300  
457 001254 177564  
458 001256 177566  
459 001260 000000  
460 001262 000000  
461 001264 000000  
462 001266 000000  
463 001270 000000  
464 001272 000000  
465 001274 000000  
466 001276 050505  
467 001300 127272  
468 001302 072727  
469 001304 105050  
470 001306 072727  
471 001310 105056  
472 001312 000000  
473 001314 000000  
474 001316 000000  
475 001320 000000  
476

TCBA: 177346  
TCDT: 177350  
TCVTR: 214  
TCLVL: 300  
TPS: 177564  
TPB: 177566  
COOCAL: OPEN  
RTNNO: OPEN  
NXTST: OPEN  
CURTST: OPEN  
CRBUF: OPEN  
CRBUFA: OPEN  
CTRA: OPEN  
SBDAT1: 50505  
SBDAT2: 72727  
SBDAT3: 72727  
POMPUS: .WORD 000000  
POMPOP: .WORD 000000  
TCMT: OPEN  
TCSTT: OPEN  
.PAGE

.SBTTL ERROR POINTER TABLE

;\*THIS TABLE CONTAINS THE INFORMATION FOR EACH ERROR THAT CAN OCCUR.  
 ;\*THE INFORMATION IS OBTAINED BY USING THE INDEX NUMBER FOUND IN  
 ;\*LOCATION SITEMB, THIS NUMBER INDICATES WHICH ITEM IN THE TABLE IS PERTINENT.  
 ;\*NOTE1: IF SITEMB IS 0 THE ONLY PERTINENT DATA IS (\$ERRPC).  
 ;\*NOTE2: EACH ITEM IN THE TABLE CONTAINS 4 POINTERS EXPLAINED AS FOLLOWS:

;\* EM ;: POINTS TO THE ERROR MESSAGE  
 ;\* DH ;: POINTS TO THE DATA HEADER  
 ;\* DT ;: POINTS TO THE DATA  
 ;\* DF ;: POINTS TO THE DATA FORMAT

\$ERRTB:

477						
478						
479						
480						
481						
482						
483						
484						
485						
486						
487						
488						
489						
490						
491	001322					
492						
493	001322	016115	EM1	;	"SAT (STOP ALL TRANSPORTS) COMMAND DID NOT CLEAR READY"	
494	001324	016203	EH1	;	" PC SP PS TEST# TCCM TCST"	
495	001326	016262	ET1	;	\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1	
496	001330	000000				
497						
498						
499	001332	016300	EM2	;	"SST (STOP SELECTED TRANSPORT) DID NOT CLEAR READY"	
500	001334	016362	EH2	;	" PC SP PS TEST# TCCM TCST"	
501	001336	016440	ET2	;	\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1	
502	001340	000000				
503						
504						
505	001342	016456	EM3	;	"READY BIT DID NOT CAUSE AN INTERRUPT"	
506	001344	016523	EH3	;	" PC SP PS TEST# TCCM TCST"	
507	001346	016602	ET3	;	\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1	
508	001350	000000				
509						
510						
511	001352	016620	EM4	;	"READY BIT CAUSED AN INTERRUPT WITH PROCESSOR AND TC11 AT SAME PRIORITY"	
512	001354	016727	EH4	;	" PC SP PS TEST# TCCM TCST"	
513	001356	017006	ET4	;	\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1	
514	001360	000000				
515						
516						
517	001362	017024	EM5	;	"TC11 FAILED TO INTERRUPT"	
518	001364	017055	EH5	;	" PC SP PS TEST# TCCM TCST"	
519	001366	017134	ET5	;	\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1	
520	001370	000000				
521						
522						
523	001372	017152	EM6	;	"TC11 DID NOT DROP INTERRUPT REQUEST AFTER IT WAS ACKNOLEDGED"	
524	001374	017247	EH6	;	" PC SP PS TEST# TCCM TCST"	
525	001376	017326	ET6	;	\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1	
526	001400	000000				
527						
528						
529	001402	017344	EM7	;	"DOING A RESET INSTRUCTION DID NOT CLEAR UPS"	
530	001404	017420	EH7	;	" PC SP PS TEST# TCCM TCST"	
531	001406	017476	ET7	;	\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1	
532	001410	000000				

533					
534					
535	001412	017514	EM10	;	"ENTERING MAINTANANCE MODE DID NOT SET UPS"
536	001414	017566	EH10	;	" PC SP PS TEST# TCCM TCST"
537	001416	017644	ET10	;	\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
538	001420	000000	000000		
539					
540					
541	001422	017662	EM11	;	"UPS DID NOT CLEAR WHEN LEAVING MAINTANANCE MODE"
542	001424	017742	EH11	;	" PC SP PS TEST# TCCM TCST"
543	001426	020020	ET11	;	\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
544	001430	000000	000000		
545					
546					
547	001432	020036	EM12	;	"TCST BIT 0 CAN BE SET WHILE IN MAINTANANCE MODE"
548	001434	020116	EH12	;	" PC SP PS TEST# TCCM TCST"
549	001436	020174	ET12	;	\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
550	001440	000000	000000		
551					
552					
553	001442	020212	EM13	;	"TCST BIT 1 CAN BE SET WHILE IN MAINTANANCE MODE"
554	001444	020272	EH13	;	" PC SP PS TEST# TCCM TCST"
555	001446	020350	ET13	;	\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
556	001450	000000	000000		
557					
558					
559	001452	020366	EM14	;	"WRM COMMAND WITH WRM SWITCH DISABLED FAILED TO SET ILO ERROR"
560	001454	020465	EH14	;	" PC SP PS TEST# TCCM TCST"
561	001456	020544	ET14	;	\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
562	001460	000000	000000		
563					
564					
565	001462	020562	EM15	;	"ILO ERROR FAILED TO SET THE 'ERROR' BIT"
566	001464	020632	EH15	;	" PC SP PS TEST# TCCM TCST"
567	001466	020710	ET15	;	\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
568	001470	000000	000000		
569					
570					
571	001472	020726	EM16	;	"CLEARING ILLEGAL OP FAILED TO CLEAR ILO ERROR"
572	001474	021004	EH16	;	" PC SP PS TEST# TCCM TCST"
573	001476	021062	ET16	;	\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
574	001500	000000	000000		
575					
576					
577	001502	021100	EM17	;	"CLEARING ILLEGAL OP FAILED TO CLEAR THE 'ERROR' BIT"
578	001504	021164	EH17	;	" PC SP PS TEST# TCCM TCST"
579	001506	021242	ET17	;	\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
580	001510	000000	000000		
581					
582					
583	001512	021260	EM20	;	"WRM WITH WRM SWITCH OFF DID NOT SET ILO ERROR BIT"
584	001514	021344	EH20	;	" PC SP PS TEST# TCCM TCST"
585	001516	021422	ET20	;	\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
586	001520	000000	000000		
587					
588					

589	001522	021440	EM21	;"ILO ERROR SETTING DID NOT CAUSE THE 'ERROR' BIT TO SET"
590	001524	021527	EH21	;" PC SP PS TEST# TCCM TCST"
591	001526	021606	ET21	;\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
592	001530	000000	000000	
593				
594				
595	001532	021624	EM22	;"CLEARING ERROR BIT ALSO CLEARED ILO ERROR"
596	001534	021676	EH22	;" PC SP PS TEST# TCCM TCST"
597	001536	021754	ET22	;\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
598	001540	000000	000000	
599				
600				
601	001542	021772	EM23	;"THE 'ERROR' BIT DID NOT SET"
602	001544	022026	EH23	;" PC SP PS TEST# TCCM TCST"
603	001546	022104	ET23	;\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
604	001550	000000	000000	
605				
606				
607	001552	022122	EM24	;"THE 'ERROR' BIT SET DID NOT CAUSE AN INTERRUPT"
608	001554	022201	EH24	;" PC SP PS TEST# TCCM TCST"
609	001556	022260	ET24	;\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
610	001560	000000	000000	
611				
612				
613	001562	022276	EM25	;"DOING A RESET INSTRUCTION DID NOT SET THE READY BIT"
614	001564	022362	EH25	;" PC SP PS TEST# TCCM TCST"
615	001566	022440	ET25	;\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
616	001570	000000	000000	
617				
618				
619	001572	022456	EM26	;"TEST EXECUTION IS OUT OF ORDER"
620	001574	022515	EH26	;" PC SP PS TEST# TEST# S/B"
621	001576	022570	ET26	;\$ERRPC, \$REG6, \$REG7, \$REG5, TEST# S/B
622	001600	000000	000000	
623				
624				
625	001602	022604	EM27	;"ERROR TRYING TO READ A BLOCK MARK"
626	001604	022646	EH27	;" PC SP PS TEST# TCCM TCST"
627	001606	022724	ET27	;\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
628	001610	000000	000000	
629				
630				
631	001612	022742	EM30	;"READY WAS NOT SET AFTER BLOCK MARK WAS SHIFTED INTO THE WINDOW REGISTE
632	001614	023052	EH30	;" PC SP PS TEST# TCCM TCST"
633	001616	023130	ET30	;\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
634	001620	000000	000000	
635				
636				
637	001622	023146	EM31	;"INCORRECT BLOCK # IN DATA REG AFTER BLOCK MARK WAS DETECTED"
638	001624	023242	EH31	;" PC SP PS TEST# TCCM TCST"
639	001626	023342	ET31	;\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
640	001630	000000	000000	
641				
642				
643	001632	023364	EM32	;"MTE WAS NOT SET BY AN ILLEGAL MARK TRACK CODE"
644	001634	023442	EH32	;" PC SP PS TEST# TCCM TCST"



701	001752	025314	EM44	:"WORD COUNT INCREMENTED IMPROPERLY"					
702	001754	025356	EH44	:" PC SP PS TEST# TCCM TCST TCWC"					
703	001756	025460	ET44	:"SERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1, TCWC"					
704	001760	000000	000000						
705									
706									
707	001762	025502	EM45	:"TCBA INCREMENTED IMPROPERLY"					
708	001764	025536	EH45	:" PC SP PS TEST# TCCM TCST TCBA"					
709	001766	025640	ET45	:"SERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1, TCBA"					
710	001770	000000	000000						
711									
712									
713	001772	025662	EM46	:"PARITY ERROR"					
714	001774	025677	EH46	:" PC SP PS TEST# TCCM TCST"					
715	001776	025756	ET46	:"SERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1"					
716	002000	000000	000000						
717									
718									
719	002002	025774	EM47	:"READY DID NOT SET AFTER READING WAS COMPLETED"					
720	002004	026052	EH47	:" PC SP PS TEST# TCCM TCST"					
721	002006	026130	ET47	:"SERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1"					
722	002010	000000	000000						
723									
724									
725	002012	026146	EM50	:"TRANSFERED TOO MANY WORDS"					
726	002014	026200	EH50	:" PC SP PS TEST# TCCM TCST RBUF+2"					
727	002016	026270	ET50	:"SERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1, RBUF+2"					
728	002020	000000	000000						
729									
730									
731	002022	026310	EM51	:"TCBA CONTAINS AN INCORRECT ADDRESS"					
732	002024	026353	EH51	:" PC SP PS TEST# TCCM TCST TCBA TCBA S/B"					
733	002026	026454	ET51	:"SERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1, TCBA TCBA S/B"					
734	002030	000000	000000						
735									
736									
737	002032	026476	EM52	:"PARRITY ERROR WAS NOT DETECTED"					
738	002034	026535	EH52	:" PC SP PS TEST# TCCM TCST"					
739	002036	026624	ET52	:"SERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1"					
740	002040	000000	000000						
741									
742									
743	002042	026644	EM53	:"PARITY ERROR DID NOT SET THE 'ERROR' BIT"					
744	002044	026715	EH53	:" PC SP PS TEST# TCCM TCST"					
745	002046	027004	ET53	:"SERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1"					
746	002050	000000	000000						
747									
748									
749	002052	027024	EM54	:"PARITY ERROR BIT WILL NOT CLEAR"					
750	002054	027064	EH54	:" PC SP PS TEST# TCCM TCST"					
751	002056	027152	ET54	:"SERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1"					
752	002060	000000	000000						
753									
754									
755	002062	027172	EM55	:"BLOCK MISS SHOULD NOT HAVE SET"					
756	002064	027231	EH55	:" PC SP PS TEST# TCCM TCST"					

757	002066	027320	ET55	;SERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
758	002070	000000	000000	
759				
760				
761	002072	027340	EM56	;"RDATA WAS ISSUED BUT BLOCK MISS FAILED TO SET"
762	002074	027416	EH56	;" PC SP PS TEST# TCCM TCST"
763	002076	027504	ET56	;SERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
764	002100	000000	000000	
765				
766				
767	002102	027524	EM57	;"BLOCK MISS SETTING DID NOT SET THE 'ERROR' BIT"
768	002104	027603	EH57	;" PC SP PS TEST# TCCM TCST"
769	002106	027672	ET57	;SERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
770	002110	000000	000000	
771				
772				
773	002112	027712	EM60	;"CLEARING ERROR BIT FAILED TO CLEAR BLOCK MISS"
774	002114	027770	EH60	;" PC SP PS TEST# TCCM TCST"
775	002116	030056	ET60	;SERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
776	002120	000000	000000	
777				
778				
779	002122	030076	EM61	;"FORWARD CHECKSUM WAS WRITTEN INCORRECTLY INTO CORE"
780	002124	030161	EH61	;" PC SP PS TEST# TCCM TCST RBUF+514"
781	002126	030260	ET61	;SERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1, RBUF+514
782	002130	000000	000000	
783				
784				
785	002132	030302	EM62	;"TWC WAS MODIFIED DURING RAL"
786	002134	030340	EH62	;" P SP PS TEST# TCCM TCST TCWC"
787	002136	030426	ET62	;SERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1, TCWC
788	002140	000000	000000	
789				
790				
791	002142	030446	EM63	;"TCBA WAS MODIFIED DURING RAL"
792	002144	030504	EH63	;" PC SP PS TEST# TCCM TCST TCBA"
793	002146	030606	ET63	;SERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1, TCBA
794	002150	000000	000000	
795				
796				
797	002152	030626	EM64	;"DATA MISS DID NOT SET"
798	002154	030654	EH64	;" PC SP PS TEST# TCCM TCST"
799	002156	030742	ET64	;SERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
800	002160	000000	000000	
801				
802				
803	002162	030762	EM65	;"DATA MISS SETTING DID NOT CAUSE THE 'ERROR' BIT TO SET"
804	002164	031051	EH65	;" PC SP PS TEST# TCCM TCST"
805	002166	031130	ET65	;SERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
806	002170	000000	000000	
807				
808				
809	002172	031146	EM66	;"CLEARING THE 'ERROR' BIT DID NOT CAUSE DATA MISS TO BE CLEARED"
810	002174	031245	EH66	;" PC SP PS TEST# TCCM TCST"
811	002176	031324	ET66	;SERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
812	002200	000000	000000	





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869
870
871 002322 012706 001100
872 002326 005026
873 002330 022706 001140
874 002334 001374
875 002336 012706 001000
876
877 002342 012737 013324 000020
878 002350 012737 000340 000022
879 002356 012737 013614 000030
880 002364 012737 000340 000032
881 002372 012737 015256 000034
882 002400 012737 000340 000036
883 002406 012737 014036 000024
884 002414 012737 000340 000026
885 002422 013737 011546 011540
886 002430 005037 001222
887 002434 005037 001224
888 002440 112737 000001 001115
889 002446 012737 002446 001106
890 002454 012737 002454 001110
891
892 002462
893
894
895 002462 013746 000004
896 002466 012737 002522 000004
897 002474 012737 177570 001140
898 002502 012737 177570 001142
899 002510 022777 177777 176422
900 002516 001012
901
902 002520 000403
903 002522 012716 002530 64$:
904 002526 000002
905 002530 012737 000176 001140 65$:
906 002536 012737 000174 001142
907 002544 012637 000004 66$:
908
909 002550 012706 001000
910 002554 005037 001262
911 002560 104401 001233
912 002564 104401 015330
913 002570 000240
914 002572 000000
915 002574 005737 000042
916 002600 001401
917 002602 000005
918 002604 005037 177776
919 002610 012706 001000
920 002614 004737 012162
921 002620 004737 012204
922 002624 000137 002630
923
924

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.SBTTL INITIALIZE THE COMMON TAGS
;; CLEAR THE COMMON TAGS ($CHTAG) AREA
MOV # $CHTAG, R6 ;; FIRST LOCATION TO BE CLEARED
CLR (R6)+ ;; CLEAR MEMORY LOCATION
CMP #SWR, R6 ;; DONE?
BNE -6 ;; LOOP BACK IF NO
MOV #1000, SP ;; SETUP THE STACK POINTER
;; INITIALIZE A FEW VECTORS
MOV # $SCOPE, @ $IOTVEC ;; IOT VECTOR FOR SCOPE ROUTINE
MOV #340, @ $IOTVEC+2 ;; LEVEL 7
MOV # $ERROR, @ $EMTVEC ;; EMT VECTOR FOR ERROR ROUTINE
MOV #340, @ $EMTVEC+2 ;; LEVEL 7
MOV # $TRAP, @ $TRAPVEC ;; TRAP VECTOR FOR TRAP CALLS
MOV #340, @ $TRAPVEC+2 ;; LEVEL 7
MOV # $PWRON, @ $PWRVEC ;; POWER FAILURE VECTOR
MOV #340, @ $PWRVEC+2 ;; LEVEL 7
MOV $ENDCT, $EOPCT ;; SETUP END-OF-PROGRAM COUNTER
CLR $TIMES ;; INITIALIZE NUMBER OF ITERATIONS
CLR $ESCAPE ;; CLEAR THE ESCAPE ON ERROR ADDRESS
MOVB #1, $SERMAX ;; ALLOW ONE ERROR PER TEST
MOV #., $SLPADR ;; INITIALIZE THE LOOP ADDRESS FOR SCOPE
MOV #., $SLPERR ;; SETUP THE ERROR LOOP ADDRESS

.LIST
SWRSU
;; SIZE FOR A HARDWARE SWITCH REGISTER. IF NOT FOUND OR IT IS
;; EQUAL TO A "-1" SETUP FOR A SOFTWARE SWITCH REGISTER.
MOV @ $ERRVEC, -(SP) ;; SAVE ERROR VECTOR
MOV #64$, @ $ERRVEC ;; SET UP ERROR VECTOR
MOV # $SWR, SWR ;; SETUP FOR A HARDWARE SWITCH REGISTER
MOV # $DISP, DISPLAY ;; AND A HARDWARE DISPLAY REGISTER
CMP # -1, @ $SWR ;; TRY TO REFERENCE HARDWARE SWR
BNE 66$ ;; BRANCH IF NO TIMEOUT TRAP OCCURRED
;; AND THE HARDWARE SWR IS NOT = -1
BR 65$ ;; BRANCH IF NO TIMEOUT
MOV #65$, (SP) ;; SET UP FOR TRAP RETURN
RTI
MOV # $SWREG, SWR ;; POINT TO SOFTWARE SWR
MOV # $DISPREG, DISPLAY
MOV (SP)+, @ $ERRVEC ;; RESTORE ERROR VECTOR
MOV #1000, SP ;; SET BOTTOM OF SP STACK.
CLR RTNNO
TYPE , $SCRLF
TYPE , $TIMES ;; PRINTOUT STARTUP MESSAGE
NOP
HALT ;; HERE IS YOUR CHANCE TO SET THE SWITCH REGISTER
STARTX: TST 42
BEQ GETROY
RESET
GETROY: CLR PSW
MOV #1000, SP ;; SET BOTTOM OF STACK.
JSR PC, $RSETT ;; ISSUE RESET.
JSR PC, $RSTMTK ;; RESTORE MARK TRACK.
JMP T0001

.SBTTL T0001
; CHECK THAT THE TCCM REGISTER CAN BE ACCESSED WITHOUT A TRAP OCCURING

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925 :*****
926 002630 000004 T0001: SCOPE
927 002632 012737 002676 000004 MOV #A0001,2#4 ;SETUP THE FATAL TRAP VECTOR
928 002640 012737 000340 000006 MOV #340,2#6 ;MAKE SURE WE GET NO INTERRUPTS IF WE TRAP
929 002646 012706 001000 MOV #1000,SP ;SETUP THE STACK POINTER
930 002652 004737 011730 JSR PC,TORDER ;MAKE SURE TESTS ARE IN PRPOER SEQUENCE
931 002656 000001 00001 ;HERE LIES THE NUMBER OF THIS TEST
932 002660 012706 001000 R0001: MOV #1000,SP ;INIT THE STACK POINTER
933 002664 005777 176350 TST @TCCM ;TRY TO READ THE TCCM
934 002670 005077 176344 CLR @TCCM ;TRY TO MODIFY THE TCCM
935 002674 000401 BR T0002 ;NO ERRORS. GO ON TO THE NEXT TEXT
936 002676 104074 A0001: ERROR 74 ;COULD NOT ACCESS TCCM
937 .SBTTL T0002
938 ;CHECK THAT THE TCST REGISTER CAN BE ACCESSED WITHOUT A TRAP OCCURING
939 :*****
940 002700 000004 T0002: SCOPE
941 002702 012737 002746 000004 MOV #A0002,2#4 ;SETUP THE FATAL TRAP VECTOR
942 002710 012737 000340 000006 MOV #340,2#6 ;MAKE SURE WE GET NO INTERRUPTS IF WE TRAP
943 002716 012706 001000 MOV #1000,SP ;SETUP THE STACK POINTER
944 002722 004737 011730 JSR PC,TORDER ;MAKE SURE TESTS ARE IN PRPOER SEQUENCE
945 002726 000002 00002 ;HERE LIES THE NUMBER OF THIS TEST
946 002730 012706 001000 R0002: MOV #1000,SP ;INIT THE STACK POINTER
947 002734 005777 176276 TST @TCST ;TRY TO READ THE TCST
948 002740 005077 176272 CLR @TCST ;TRY TO MODIFY THE TCST
949 002744 000401 BR T0003 ;NO ERRORS. GO ON TO THE NEXT TEXT
950 002746 104075 A0002: ERROR 75 ;COULD NOT ACCESS TCST
951 ;CHECK THAT THE TCWC REGISTER CAN BE ACCESSED WITHOUT A TRAP OCCURING
952 .SBTTL T0003
953 :*****
954 002750 000004 T0003: SCOPE
955 002752 012737 003016 000004 MOV #A0003,2#4 ;SETUP THE FATAL TRAP VECTOR
956 002760 012737 000340 000006 MOV #340,2#6 ;MAKE SURE WE GET NO INTERRUPTS IF WE TRAP
957 002766 012706 001000 MOV #1000,SP ;SETUP THE STACK POINTER
958 002772 004737 011730 JSR PC,TORDER ;MAKE SURE TESTS ARE IN PRPOER SEQUENCE
959 002776 000003 00003 ;HERE LIES THE NUMBER OF THIS TEST
960 003000 012706 001000 R0003: MOV #1000,SP ;INIT THE STACK POINTER
961 003004 005777 176232 TST @TCWC ;TRY TO READ THE TCWC
962 003010 005077 176226 CLR @TCWC ;TRY TO MODIFY THE TCWC
963 003014 000401 BR T0004 ;NO ERRORS. GO ON TO THE NEXT TEXT
964 003016 104076 A0003: ERROR 76 ;COULD NOT ACCESS TCWC
965 ;CHECK THAT THE TCBA REGISTER CAN BE ACCESSED WITHOUT A TRAP OCCURING
966 .SBTTL T0004
967 :*****
968 003020 000004 T0004: SCOPE
969 003022 012737 003066 000004 MOV #A0004,2#4 ;SETUP THE FATAL TRAP VECTOR
970 003030 012737 000340 000006 MOV #340,2#6 ;MAKE SURE WE GET NO INTERRUPTS IF WE TRAP
971 003036 012706 001000 MOV #1000,SP ;SETUP THE STACK POINTER
972 003042 004737 011730 JSR PC,TORDER ;MAKE SURE TESTS ARE IN PRPOER SEQUENCE
973 003046 000004 00004 ;HERE LIES THE NUMBER OF THIS TEST
974 003050 012706 001000 R0004: MOV #1000,SP ;INIT THE STACK POINTER
975 003054 005777 176164 TST @TCBA ;TRY TO READ THE TCBA
976 003060 005077 176160 CLR @TCBA ;TRY TO MODIFY THE TCBA
977 003064 000401 BR T0005 ;NO ERRORS. GO ON TO THE NEXT TEXT
978 003066 104077 A0004: ERROR 77 ;COULD NOT ACCESS TCBA
979
980 ;CHECK THAT ISSUING A SAT COMMAND (STOP ALL TRANSPORTS) CAUSES READY BIT

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981 ;TO CLEAR IMMEDIATELY (TCCM BIT 7).
982 .SBTTL T0005
983 *****
984 T0005: SCOPE
985     MOV     #TRAP4,4           ;SETUP FATAL TRAP VECTORS
986     MOV     #TRAP10,10
987     MOV     #340,6
988     MOV     #340,12
989     MOV     #1000,SP         ;SETUP THE STACK POINTER
990     JSR     PC,TORDER        ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
991     00005                    ;HERE LIES THE NUMBER OF THIS TEST
992     MOV     TCCM,RO          ;TCCM ADDR TO RO.
993     CLR     (0)              ;SELECT UD, FUNCTION 0. (SAT COMMAND).
994     INC     (0)              ;DO.
995     TSTB   (0)              ;SEE IF READY IS SET.
996     BPL    A0005            ;BR IF READY NOT SET. (OK).
997     ERROR 1                  ;SAT COMMAND FAILED TO CLEAR READY.
998
999     MOV     #1000,SP         ;RESTORE THE STACK POINTER
1000    BR     T0006            ;GO ON TO THE NEXT TEST
1001 ;CHECK THAT ISSUING SST COMMAND (STOP SELECTED TRANSPORT) CAUSES READY
1002 ;BIT TO CLEAR IMMEDIATELY (TCCM BIT 7)
1003 .SBTTL T0006
1004 *****
1005 T0006: SCOPE
1006     MOV     #1000,SP         ;SETUP THE STACK POINTER
1007     JSR     PC,TORDER        ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
1008     00006                    ;HERE LIES THE NUMBER OF THIS TEST
1009     MOV     TCCM,RO          ;TCCM ADDR TO RO.
1010     MOV     #10,(0)         ;SELECT UD,FUNCTION 100. (SST COMMAND).
1011     INC     (0)              ;DO.
1012     TSTB   (0)              ;SEE IF READY IS SET.
1013     BPL    A0006            ;BR IF READY NOT SET. (OK).
1014     ERROR 2                  ;SST COMMAND FAILED TO CLEAR READY.
1015
1016     MOV     #1000,SP         ;RESTORE THE STACK POINTER
1017     BR     T0007            ;GO ON TO THE NEXT TEST
1018 ;TEST THAT READY BIT CAN CAUSE AN INTERRUPT. IF THE INTERRUPT IS SERVICED,
1019 ;IT WILL HAVE OCCURRED AT THE CORRECT VECTOR.
1020 .SBTTL T0007
1021 *****
1022 T0007: SCOPE
1023     MOV     #1000,SP         ;SETUP THE STACK POINTER
1024     JSR     PC,TORDER        ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
1025     00007                    ;HERE LIES THE NUMBER OF THIS TEST
1026     JSR     PC,STTCV         ;SET INTERRUPT VECTOR TO CB.
1027     A0007                    ;
1028     CLR     @TCCM            ;DISABLE TC11 INTERRUPTS.
1029     CLR     PSW              ;SET PROCESSOR PRIORITY 0.
1030     BIS    #BIT6,@TCCM      ;ENABLE TC11 INTERRUPTS.
1031     NOP
1032     ERROR 3                  ;READY DID NOT INTERRUPT.
1033
1034     MOV     #1000,SP         ;RESTORE THE STACK POINTER
1035     BR     T0010            ;GO ON TO THE NEXT TEST
1036 ;TEST THAT READY DOES NOT CAUSE INTERRUPT WITH PROCESSOR AT SAME PRIORITY

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1037 ;LEVEL AS THE TC11 INTERRUPT PRIORITY.
1038 .SBTTL T0010
1039 *****
1040 003274 000004          T0010: SCOPE
1041 003276 012706 001000      MOV      #1000,SP      ;SETUP THE STACK POINTER
1042 003302 004737 011730      JSR      PC,TORDER    ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
1043 003306 000010          00010      ;HERE LIES THE NUMBER OF THIS TEST
1044 003310 004737 012136      RO010:   JSR      PC,STTCV    ;SET INTERRUPT VECTOR TO DC.
1045 003314 003352          BO010
1046 003316 013737 001252 177776  MOV      TCLVL,PSW    ;SET PROCESSOR TO SAME PRTY AS TC11.
1047 003324 005077 175710      CLR      @TCCM        ;DISABLE TC11 INTERRUPTS.
1048 003330 052777 000100 175702  BIS      #BIT6,@TCCM  ;ENABLE TC11 INTERRUPTS.
1049 003336 000240          NOP
1050 003340 005077 175674      AO010:   CLR      @TCCM      ;DISABLE TC11 INTERRUPTS. (OK).
1051
1052 003344 012706 001000      MOV      #1000,SP    ;RESTORE THE STACK POINTER
1053 003350 000402          BR       T0011       ;GO ON TO THE NEXT TEST
1054 003352 104000          BO010:   ERROR      ;HERE IF INT. OCCURS.
1055                                     ;TC11 INTERRUPTED, WITH PROCESSOR AT SAME
1056 003354 000771          BR       AO010       ;PRTY AS TC11 INTERRUPT PRTY.
1057 ;TEST THAT TC11 INTERRUPTS WHEN PROCESSOR IS AT PRIORITY ONE LEVEL LOWER
1058 ;THAN THE TC11 INTERRUPT PRIORITY.
1059 .SBTTL T0011
1060 *****
1061 003356 000004          T0011:   SCOPE
1062 003360 012706 001000      MOV      #1000,SP    ;SETUP THE STACK POINTER
1063 003364 004737 011730      JSR      PC,TORDER    ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
1064 003370 000011          00011      ;HERE LIES THE NUMBER OF THIS TEST
1065 003372 004737 012136      RO011:   JSR      PC,STTCV    ;SET INTERRUPT VECTOR TO EB.
1066 003376 003434          AO011
1067 003400 005077 175634      CLR      @TCCM        ;DISABLE TC11 INTERRUPTS.
1068 003404 013737 001252 177776  MOV      TCLVL,PSW    ;SET PROCESSOR TO PRTY ONE LEVEL LOWER
1069 003412 162737 000040 177776  SUB      #40,PSW      ;THAN TC11 INTERRUPT PRTY.
1070 003420 052777 000100 175612  BIS      #BIT6,@TCCM  ;ENABLE TC11 INTERRUPTS.
1071 003426 000240          NOP
1072 003430 104003          ERROR 3      ;TC11 FAILED TO INT. WITH PROCESSOR AT
1073 003432 000401          BR       BO011       ;PRTY ONE LEVEL LOWER THAN TC11 INT. PRTY.
1074 003434 022626          AO011:   POPSP2      ;HERE IF INT. OCCURS. POP STACK TWICE.
1075 003436 005077 175576      BO011:   CLR      @TCCM      ;DISABLE TC11 INTERRUPTS.
1076
1077 003442 012706 001000      MOV      #1000,SP    ;RESTORE THE STACK POINTER
1078 003446 000400          BR       T0012       ;GO ON TO THE NEXT TEST
1079
1080 ;TEST TC11 DOES NOT REINTERRUPT AFTER INITIAL INTERRUPT HAS BEEN SERVICED.
1081 .SBTTL T0012
1082 *****
1083 003450 000004          T0012:   SCOPE
1084 003452 012706 001000      MOV      #1000,SP    ;SETUP THE STACK POINTER
1085 003456 004737 011730      JSR      PC,TORDER    ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
1086 003462 000012          00012      ;HERE LIES THE NUMBER OF THIS TEST
1087 003464 004737 012136      RO012:   JSR      PC,STTCV    ;SET INTERRUPT VECTOR TO FC.
1088 003470 003526          BO012
1089 003472 005077 175542      CLR      @TCCM        ;DISABLE TC11 INTERRUPTS.
1090 003476 005037 177776      CLR      PSW          ;SET PROCESSOR PRTY 0.
1091 003502 052777 000100 175530  BIS      #BIT6,@TCCM  ;ENABLE TC11 INTERRUPTS.
1092 003510 000240          NOP
    
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1093 003512 104005
1094 003514 005077 175520 R0012: CLR 5 ;TC11 FAILED TO INTERRUPT.
;DISABLE TC11 INTERRUPTS.
1095
1096 003520 012706 001000 MOV #1000,SP ;RESTORE THE STACK POINTER
1097 003524 000413 BR T0013 ;GO ON TO THE NEXT TEST
1098 003526 012777 003546 175514 B0012: MOV #00012,@TCVTR ;CHANGE INT POINTER TO FE.
1099 003534 012716 003542 MOV #C0012,@SP ;CHANGE INT EXIT POINTER TO FD.
1100 003540 000002 RTI ;EXIT INTERRUPT
1101 003542 000240 C0012: NOP ;OK IF NO INT. REOCCURS.
1102 003544 000763 BR A0012
1103 003546 022626 D0012: POPSP2 ;HERE IF REINTERRUPT OCCURS.
1104 003550 104006 ERROR 6 ;TC11 REINTERRUPTED AFTER RTI.
1105 003552 000760 BR A0012
1106 ;TEST THAT SETTING MAINTENANCE BIT (TCCM BIT 13) SETS UPS BIT (TCST BIT 7)
1107 ;THAT CLEARING MAINTENANCE BIT CLEARS UPS, AND THAT RESET CLEARS UPS.
1108 .SBTTL T0013
1109 *****
1110 003554 000004 T0013: SCOPE
1111 003556 012706 001000 MOV #1000,SP ;SETUP THE STACK POINTER
1112 003562 004737 011730 JSR PC,T0013 ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
1113 003566 000013 00013 ;HERE LIES THE NUMBER OF THIS TEST
1114 003570 032777 000200 175440 R0013: BIT #BIT7,@TCST ;SEE IF UPS IS CLEAR.
1115 003576 001402 BEQ A0013 ;BR IF UPS IS CLEAR.
1116 003600 104007 ERROR 7 ;RESET FAILED TO CLEAR UPS.
1117 003602 000421 BR C0013
1118 003604 052777 020000 175426 A0013: BIS #BIT13,@TCCM ;SET MAINTENANCE BIT.
1119 003612 032777 000200 175416 BIT #BIT7,@TCST ;SEE IF UPS IS SET.
1120 003620 001002 BNE B0013 ;BR IF UPS IS SET.
1121 003622 104010 ERROR 10 ;MAINT BIT FAILED TO SET UPS.
1122 003624 000410 BR C0013
1123 003626 042777 020000 175404 B0013: BIC #BIT13,@TCCM ;CLEAR MAINT BIT.
1124 003634 032777 000200 175374 BIT #BIT7,@TCST ;SEE IF UPS IS CLEAR.
1125 003642 001401 BEQ C0013 ;BR IF UPS IS CLEAR.
1126 003644 104011 ERROR 11 ;CLEARING MAINT. BIT FAILED TO CLEAR UPS.
1127 003646 052777 020000 175364 C0013: BIS #BIT13,@TCCM ;SET MAINT BIT TO SET UPS.
1128 003654 004737 012162 JSR PC,SRSETT ;ISSUE RESET TO CLEAR MAINT AND UPS BITS.
1129
1130 003660 012706 001000 MOV #1000,SP ;RESTORE THE STACK POINTER
1131 003664 000400 BR T0014 ;GO ON TO THE NEXT TEST
1132 ;TEST THAT SETTING MAINT. BIT DISABLES LOADING XD16 (TCST BIT 0).
1133 .SBTTL T0014
1134 *****
1135 003666 000004 T0014: SCOPE
1136 003670 012706 001000 MOV #1000,SP ;SETUP THE STACK POINTER
1137 003674 004737 011730 JSR PC,T0014 ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
1138 003700 000014 00014 ;HERE LIES THE NUMBER OF THIS TEST
1139 003702 052777 020000 175330 R0014: BIS #BIT13,@TCCM ;SET MAINTENANCE BIT.
1140 003710 052777 000001 175320 BIS #BIT0,@TCST ;TRY SETTING XD16.
1141 003716 032777 000001 175312 BIT #BIT0,@TCST ;SEE IF XD16 IS SET.
1142 003724 001401 BEQ A0014 ;BR IF XD16 IS CLEAR.
1143 003726 104012 ERROR 12 ;MAINT BIT SET FAILS TO PREVENT LOADING
1144 003730 004737 012162 A0014: JSR PC,SRSETT ;OF XD16.
1145
1146 003734 012706 001000 MOV #1000,SP ;RESTORE THE STACK POINTER
1147 003740 000400 BR T0015 ;GO ON TO THE NEXT TEST
1148 ;TEST THAT SETTING MAINT. BIT DISABLES LOADING XD17 (TCST BIT 1).

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# E03

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 T0015

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1149 .SBTTL T0015
1150 *****
1151 003742 000004 T0015: SCOPE
1152 003744 012706 001000 MOV #1000,SP ;SETUP THE STACK POINTER
1153 003750 004737 011730 JSR PC,TORDER ;MAKE SURE TESTS ARE IN PRPOER SEQUENCE
1154 003754 000015 00015 ;HERE LIES THE NUMBER OF THIS TEST
1155 003756 052777 020000 175254 R0015: BIS #BIT13,@TCCM ;SET MAINTENANCE BIT.
1156 003764 052777 000002 175244 BIS #BIT1,@TCST ;TRY SETTING XD17.
1157 003772 032777 000002 175236 BIT #BIT1,@TCST ;SEE IF XD17 IS SET.
1158 004000 001401 BEQ A0015 ;BR IF XD17 IS CLEAR.
1159 004002 104013 ERROR 13 ;MAINT BIT FAILED TO PREVENT SETTING
1160 004004 004737 012162 A0015: JSR PC,SRSETT ;OF XD17.
1161
1162 004010 012706 001000 MOV #1000,SP ;RESTORE THE STACK POINTER
1163 004014 000400 BR T0016 ;GO ON TO THE NEXT TEST
1164
1165 ;CHECK THAT ISSUING WRTH COMMAND WITH WRTH SWITCH OFF CAUSES AN ILO ERROR.
1166 ;(ILLEGAL OP- TCST BIT 12), AND THAT ERROR BIT SETS. ;(TCCM BIT 15).
1167 ;TEST DONE WITH MAINTENANCE BIT SET.
1168 .SBTTL T0016
1169 *****
1170 004016 000004 T0016: SCOPE
1171 004020 012706 001000 MOV #1000,SP ;SETUP THE STACK POINTER
1172 004024 004737 011730 JSR PC,TORDER ;MAKE SURE TESTS ARE IN PRPOER SEQUENCE
1173 004030 000016 00016 ;HERE LIES THE NUMBER OF THIS TEST
1174 004032 012777 020012 175200 R0016: MCV #MAINT!FWD!UO!WRTH,@TCCM
1175 004040 000240 NOP
1176 004042 032777 010000 175166 BIT #BIT12,@TCST ;SEE IF ILO ERROR IS SET.
1177 004050 001002 BNE A0016 ;BR IF ILO ERR IS SET.
1178 004052 104014 ERROR 14 ;WRTH COMMAND WITH WRTH SWITCH DISABLED
1179 004054 000421 BR D0016 ;FAILED TO SET ILO ERROR.
1180 004056 005777 175156 A0016: TST @TCCM ;SEE IF ERROR BIT IS SET.
1181 004062 100402 BMI B0016 ;BR IF ERROR BIT IS SET.
1182 004064 104015 ERROR 15 ;ILO ERR FAILED TO SET ERROP BIT.
1183 004066 000414 BR D0016
1184 004070 005077 175144 B0016: CLR @TCCM ;CLEAR ILLEGAL COMMAND.
1185 004074 032777 010000 175134 BIT #BIT12,@TCST ;SEE IF ILO ERROR IS SET.
1186 004102 001402 BEQ C0016 ;BR IF ILO ERROR IS CLEAR.
1187 004104 104016 ERROR 16 ;CLEARING ILLEGAL OP FAILED TO CLEAR
1188 004106 000404 BR D0016 ;ILO ERROR.
1189 004110 005777 175124 C0016: TST @TCCM ;SEE IF ERROR BIT IS CLEAR.
1190 004114 100001 BPL D0016 ;BR IF ERROR IS CLEAR.
1191 004116 104017 ERROR 17 ;CLEARING ILLEGAL OP FAILED TO
1192 004120 004737 012162 D0016: JSR PC,SRSETT ;CLEAR ERROR BIT.
1193
1194 004124 012706 001000 MOV #1000,SP ;RESTORE THE STACK POINTER
1195 004130 000400 BR T0017 ;GO ON TO THE NEXT TEST
1196
1197 ;CHECK THAT ISSUING WRTH COMMAND (WRITE TIMING AND MARK) WITH WRTH SWITCH
1198 ;OFF CAUSES AN ILO ERROR(ILLEGAL OP- TCST BIT 12) AND THAT ERROR BIT SETS.
1199 ;(TCCM BIT 15). TEST DONE WITH MAINTENANCE BIT SET.
1200 .SBTTL T0017
1201 *****
1201 004132 000004 T0017: SCOPE
1202 004134 012706 001000 MOV #1000,SP ;SETUP THE STACK POINTER
1203 004140 004737 011730 JSR PC,TORDER ;MAKE SURE TESTS ARE IN PRPOER SEQUENCE
1204 004144 000017 00017 ;HERE LIES THE NUMBER OF THIS TEST

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# F03

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1205 004146 012777 020012 175064 R0017: MOV #MAINT!FWD!UO!WRTM,@TCCM
1206 004154 000240 NOP
1207 004156 032777 010000 175052 BIT #BIT12,@TCST ;SEE IF ILO ERR IS SET.
1208 004164 001002 BNE R0017 ;BR IF ILO SET.
1209 004166 104020 ERROR 20 ;WRTM WITH WRTM SW OFF FAILED TO SET
1210 004170 000421 BR D0017 ;ILO ERROR.
1211 004172 005777 175042 A0017: TST @TCCM ;ERROR BIT SET?
1212 004176 100402 BMI B0017 ;BR IF ERROR BIT SET.
1213 004200 104021 ERROR 21 ;ERROR BIT NOT SET WITH ILO ERR SET.
1214 004202 000414 BR D0017
1215 004204 005077 175030 B0017: CLR @TCCM ;CLEAR ILLEGAL COMMAND.
1216 004210 032777 010000 175020 BIT #BIT12,@TCST ;SEE IF ILO ER IS CLEAR.
1217 004216 001402 BEQ C0017 ;BR ID ILO ERR IS CLEAR.
1218 004220 104016 ERROR 16 ;CLEARING ILLEGAL OP FAILED TO
1219 004222 000404 BR D0017 ;CLEAR ILO ERR.
1220 004224 005777 175010 C0017: TST @TCCM ;ERROR BIT SET?
1221 004230 100001 BPL D0017 ;BR IF ERROR BIT IS CLEAR.
1222 004232 104017 ERROR 17 ;CLEARING ILLEGAL OP FAILED TO
1223 004234 004737 012162 D0017: JSR PC,SRSET* ;CLEAR ERROR BIT.
1224
1225 004240 012706 001000 MOV #1000,SP ;RESTORE THE STACK POINTER
1226 004244 000400 BR T0020 ;GO ON TO THE NEXT TEST
1227
1228 ;TEST THAT CLEARING ERROR BIT DOES NOT CLEAR ILO ERROR.
1229 .SBTTL T0020
1230 *****
1231 004246 000004 T0020: SCOPE
1232 004250 012706 001000 MOV #1000,SP ;SETUP THE STACK POINTER
1233 004254 004737 011730 JSR PC,TORDER ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
1234 004260 000020 D0020 ;HERE LIES THE NUMBER OF THIS TEST
1235 004262 012777 020012 174750 R0020: MOV #MAINT!FWD!UO!WRTM,@TCCM
1236 004270 000240 NOP
1237 004272 005777 174742 TST @TCCM ;ERROR SET?
1238 004276 100402 BMI A0020 ;BR IF ERROR BIT IS SET.
1239 004300 104023 ERROR 23 ;ERROR BIT FAILED TO SET.
1240 004302 000410 BR B0020
1241 004304 042777 100000 174726 A0020: BIC #BIT15,@TCCM ;TRY CLEARING ERROR BIT.
1242 004312 032777 010000 174716 BIT #BIT12,@TCST ;ILO SET?
1243 004320 001001 BNE B0020 ;BR IF ILO IS SET.
1244 004322 104022 ERROR 22 ;0 TO ERROR BIT CLEARED ILO ERROR.
1245 004324 004737 012162 B0020: JSR PC,SRSETT ;RESET.
1246
1247 004330 012706 001000 MOV #1000,SP ;RESTORE THE STACK POINTER
1248 004334 000400 BR T0021 ;GO ON TO THE NEXT TEST
1249 ;TEST THAT ERROR BIT (TCCM BIT15) IS ABLE TO CAUSE AN INTERRUPT.
1250 .SBTTL T0021
1251 *****
1252 004336 000004 T0021: SCOPE
1253 004340 012706 001000 MOV #1000,SP ;SETUP THE STACK POINTER
1254 004344 004737 011730 JSR PC,TORDER ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
1255 004350 000021 D0021 ;HERE LIES THE NUMBER OF THIS TEST
1256 004352 004737 012136 R0021: JSR PC,STTCV ;SET TC11 INT. VECTOR TO MB.
1257 004356 004404 A0021
1258 004360 005077 174654 CLR @TCCM ;DISABLE TC11 INTERRUPTS.
1259 004364 005037 177776 CLR PSW ;SET PRY 0.
1260 004370 052777 000100 174642 BIS #BIT6,@TCCM ;ENABLE TC11 INTERRUPTS.
  
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1261 004376 000240      NOP
1262 004400 104005      ERROR 5          ;TC11 FAILED TO INTERRUPT.
1263 004402 000415      BR              D0021
1264 004404 012777 004434 174636 A0021: MOV      #C0021,@TCVTR ;CHANGE INT VECTOR TO MD.
1265 004412 012716 004420      MOV      #B0021,@SP  ;CHANGE INT EXIT POINTER TO MC.
1266 004416 000002      RTI           ;EXIT INTERRUPT.
1267 004420 052777 020012 174612 B0021: BIS      #MAINT!FWD!UO!WRTH,@TCCM
1268 004426 000240      NOP
1269 004430 104024      ERROR 24        ;ERROR BIT FAILED TO INTERRUPT.
1270 004432 000401      BR              D0021
1271 004434 022626      C0021: POPSP2      ;HERE IF ERROR INTERRUPTS.
1272 004436 005077 174576 D0021: CLR      @TCCM    ;DISABLE INT. CLEAR ILLEGAL OP.
1273
1274 004442 012706 001000      MOV      #1000,SP  ;RESTORE THE STACK POINTER
1275 004446 000400      BR              T0022 ;GO ON TO THE NEXT TEST
1276
1277
1278 ;TEST THAT ISSUING RNUM COMMAND (READ BLOCK #) CLEARS READY BIT.
1279 ;RESET INSTRUCTION SHOULD SET READY. TEST DONE WITH MAINT. BIT SET.
1280 .SBTTL T0022
1281 *****
1281 004450 000004      T0022: SCOPE
1282 004452 012706 001000      MOV      #1000,SP  ;SETUP THE STACK POINTER
1283 004456 004737 011730      JSR      PC,TORDER ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
1284 004462 000022      00022      ;HERE LIES THE NUMBER OF THIS TEST
1285 004464 105777 174550 R0022: TSTB     @TCCM    ;READY SET?
1286 004470 100402      BMI      A0022     ;BR IF READY IS SET.
1287 004472 104025      ERROR 25        ;RESET DID NOT FORCE READY TO SET.
1288 004474 000407      BR              B0022
1289 004476 012777 020703 174534 A0022: MOV      #MAINT!UO!FWD!RNUM!DO,@TCCM
1290 004504 105777 174530      TSTB     @TCCM    ;READY CLEAR?
1291 004510 100001      BPL      B0022     ;BR IF READY IS CLEAR.
1292 004512 104076      ERROR 76        ;RNUM,DO, FAILED TO CLEAR READY.
1293 004514 004737 012162 B0022: JSR      PC,SRSETT ;ISSUE RESET TO FORCE READY TO SET.
1294
1295 004520 012706 001000      MOV      #1000,SP  ;RESTORE THE STACK POINTER
1296 004524 000400      BR              T0023 ;GO ON TO THE NEXT TEST
1297
1298 ;TEST THAT TC11 CONTROL CAN RECOGNIZE A BLOCK MARK. WITH MAINT BIT SET,
1299 ;RNUM COMMAND IS ISSUED. A SUBROUTINE PROVIDES TIMING AND MARK DATA.
1300 ;WHEN THE BLOCK MARK HAS BEEN SHIFTED INTO THE WINDOW, THE READY BIT SHOULD SET.
1301 .SBTTL T0023
1302 *****
1302 004526 000004      T0023: SCOPE
1303 004530 012706 001000      MOV      #1000,SP  ;SETUP THE STACK POINTER
1304 004534 004737 011730      JSR      PC,TORDER ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
1305 004540 000023      00023      ;HERE LIES THE NUMBER OF THIS TEST
1306 004542 005077 174472 R0023: CLR      @TCCM
1307 004546 012777 020003 174464      MOV      #MAINT!UO!FWD!RNUM!DO,@TCCM
1308 004554      MTCOD      MTK7,6
1309 004554 004537 012636      JSR      R5,LATCOD ;CALL LOAD MT CODES SUB.
1310 004560 033164      MTK7
1311 004562 000006      6          ;ADDRESS OF MARK TRACK CODES.
1312 004564 005777 174450      TST      @TCCM    ;MARK TRACK CODE COUNT.
1313 004570 100002      BPL      ALJ23     ;ERROR BIT SET?
1314 004572 104027      ERROR 27        ;BR IF NO ERROR.
1315 004574 000404      BR              B0023 ;ERROR BIT SET. EXAMINE TCST OR LIGHT PANEL.
1316 004576 105777 174436 A0023: TSTB     @TCCM    ;READY BIT SET?

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T0023

1317 004602 100401  
1318 004604 104030  
1319  
1320  
1321  
1322  
1323 004606  
1324 004606 012706 001000  
1325 004612 000400  
1326  
1327  
1328  
1329  
1330  
1331  
1332 004614 000004  
1333 004616 012706 001000  
1334 004622 004737 011730  
1335 004626 000024  
1336 004630 005077 174404  
1337 004634 012777 020003 174376  
1338 004642  
1339 004642 004537 012636  
1340 004646 033164  
1341 004650 000006  
1342 004652 022777 052525 174366  
1343 004660 001415  
1344 004662 017737 174360 001172  
1345 004670 012737 052525 001162  
1346 004676 017737 174344 001172  
1347 004704 012737 052525 001162  
1348 004712 104031  
1349 004714  
1350 004714 012706 001000  
1351 004720 000400  
1352  
1353  
1354  
1355  
1356  
1357 004722 000004  
1358 004724 012706 001000  
1359 004730 004737 011730  
1360 004734 000025  
1361 004736 004537 012610  
1362 004742 033134  
1363 004744 033236  
1364 004746 000006  
1365 004750 012777 020003 174262  
1366 004756  
1367 004756 004537 012636  
1368 004762 033164  
1369 004764 000011  
1370 004766 032777 020000 174242  
1371 004774 001002  
1372 004776 104032

BMI B0023 ; BR IF READY IS SET.  
ERROR 30 ; READY NOT SET AFTER BLOCK MARK WAS  
; SHIFTED INTO WINDOW REG WITH RNUM COMMAND  
; IN EFFECT. EVERYTHING IS SUSPECT AT THIS  
; POINT. ABILITY TO SHIFT TIMING AND MARK  
; DATA WHILE IN MAINT MODE HAS NOT BEEN  
B0023: ;  
MOV #1000,SP ; RESTORE THE STACK POINTER  
BR T0024 ; GO ON TO THE NEXT TEST  
; TEST THAT TC11 CONTROL TRANSFERS THE BLOCK NUMBER TO THE DATA REGISTER  
; WHEN BLOCK MARK IS DETECTED AND CONTROL IS DOING RNUM COMMAND. A SUBROUTINE  
; PROVIDES TIMING, MARK, AND DATA. WHEN THE READY BIT SETS, THE BLOCK #  
; EXPECTED IN THE DATA REGISTER IS 000525.  
; SBTTL T0024  
; \*\*\*\*\*  
T0024: SCOPE  
MOV #1000,SP ; SETUP THE STACK POINTER  
JSR PC,TORDER ; MAKE SURE TESTS ARE IN PROPER SEQUENCE  
00024 ; HERE LIES THE NUMBER OF THIS TEST  
R0024: CLR @TCCM  
MOV #MAINT!UO!FWD!RNUM!DO,@TCCM  
MTCOD MTK7,6  
JSR RS,LATCOD ; CALL LOAD MT CODES SUB.  
MTK7 ; ADDRESS OF MARK TRACK CODES.  
6 ; MARK TRACK CODE COUNT.  
CMP #52525,@TCDT ; TCDT=52525?  
BEQ R0024 ; BR IF TCDT CORRECT.  
MOV @TCDT,\$REG4 ; SETUP BLOBK # FOR PRINTOUT  
MOV #52525,\$REG0 ; SETUP GOOD BLOBK # TO PRINTOUT  
MOV @TCDT,\$REG4 ; SETUP BLOBK # FOR PRINTOUT  
MOV #52525,\$REG0 ; SETUP GOOD BLOBK # TO PRINTOUT  
ERROR 31 ; ERROR. BLOBK # IN TCDT NOT 52525. EXAMINE TCDT.  
R0024: MOV #1000,SP ; RESTORE THE STACK POINTER  
BR T0025 ; GO ON TO THE NEXT TEST  
; TEST THAT TC11 CONTROL IS ABLE TO DETECT AN INCORRECT MARK TRACK CODE.  
; A SUBROUTINE PROVIDES TIMING AND MARK DATA WHILE CONTROL IS IN RNUM  
; COMMAND. WHEN THE INCORRECT MARK IS SHIFTED, THE MTE AND ERR BITS SHOULD SET.  
; SBTTL T0025  
; \*\*\*\*\*  
T0025: SCOPE  
MOV #1000,SP ; SETUP THE STACK POINTER  
JSR PC,TORDER ; MAKE SURE TESTS ARE IN PROPER SEQUENCE  
00025 ; HERE LIES THE NUMBER OF THIS TEST  
R0025: JSR RS,BMOVE ; SET INVALID CODE IN MARK TRACK.  
MTKER  
MTKVAR  
6  
MOV #MAINT!UO!FWD!RNUM!DO,@TCCM  
MTCOD MTK7,9  
JSR RS,LATCOD ; CALL LOAD MT CODES SUB.  
MTK7 ; ADDRESS OF MARK TRACK CODES.  
9 ; MARK TRACK CODE COUNT.  
BIT #BIT13,@TGST ; MTE BIT SET? (MARK TRACK ERROR).  
BNE R0025 ; BR IF MTE BIT IS SET.  
ERROR 32 ; INVALID MARK TRACK CODE FAILED TO SET MTE.

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T0025

1373	005000	000404	
1374	005002	005777	174232
1375	005006	100401	
1376	005010	104033	
1377	005012		
1378	005012	012706	001000
1379	005016	000400	
1380			
1381			
1382			
1383			
1384			
1385	005020	000004	
1386	005022	012706	001000
1387	005026	004737	011730
1388	005032	000026	
1389	005034	004537	012610
1390	005040	033142	
1391	005042	033214	
1392	005044	000006	
1393	005046	012777	020003 174164
1394	005054		
1395	005054	004537	012636
1396	005060	033164	
1397	005062	000005	
1398	005064	005777	174146
1399	005070	100402	
1400	005072	104034	
1401	005074	000404	
1402	005076	005777	174136
1403	005102	100401	
1404	005104	104035	
1405	005106		
1406	005106	012706	001000
1407	005112	000400	
1408			
1409			
1410			
1411			
1412	005114	000004	
1413	005116	012706	001000
1414	005122	004737	011730
1415	005126	000027	
1416	005130	004537	012610
1417	005134	033150	
1418	005136	033214	
1419	005140	000006	
1420	005142	005077	174072
1421	005146	012777	020003 174064
1422	005154		
1423	005154	004537	012636
1424	005160	033164	
1425	005162	000005	
1426	005164	005777	174046
1427	005170	100002	
1428	005172	104036	

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A0025: BR      B0025
        TST     @TCCM      ;ERROR BIT SET?
        BMI     B0025      ;BR IF ERROR BIT IS SET.
        ERROR 33          ;MTE BIT FAILED TO SET ERROR BIT.

B0025: MOV     #1000,SP    ;RESTORE THE STACK POINTER
        BR      T0026     ;GO ON TO THE NEXT TEST
;TEST THAT TC11 CONTROL DETECTS END ZONE MARK CODES. A SUBROUTINE PROVIDES
;TIMING AND MARK DATA WHILE CONTROL IS IN RNUM COMMAND. WHEN THE ENDZ
;MARK CODE IS SHIFTED INTO THE WINDOW, THE ENDZ AND ERROR BITS SHOULD SET.
.SBTL T0026
;*****
T0026: SCOPE
        MOV     #1000,SP    ;SETUP THE STACK POINTER
        JSR    PC,TORDER   ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
        00026             ;HERE LIES THE NUMBER OF THIS TEST
R0026: JSR    RS,BMOVE     ;SET END CODE IN MARK TRACK.
        MTKEND
        MTK5
        6
        MOV     #MAINT!UD!FWD!RNUM!DO,@TCCM
        MTCOD  MTK7,5
        JSR    RS,LATCOD   ;CALL LOAD MT CODES SUB.
        MTK7             ;ADDRESS OF MARK TRACK CODES.
        5                ;MARK TRACK CODE COUNT.
        TST     @TCST      ;ENDZ BIT SET?
        BMI     A0026      ;BR IF ENDZ BIT IS SET.
        ERROR 34          ;ENDZ MARK FAILED TO SET ENDZ BIT.

A0026: TST     @TCCM      ;ERROR BIT SET?
        BMI     B0026      ;BR IF ERROR BIT IS SET.
        ERROR 35          ;ENDZ BIT FAILED TO SET ERROR BIT.

B0026: MOV     #1000,SP    ;RESTORE THE STACK POINTER
        BR      T0027     ;GO ON TO THE NEXT TEST
;TEST THAT TC11 CONTROL DOES NOT RECOGNIZE MARK TRACK CODE 55 AS END ZONE
;BLOCK MARK. SUBROUTINE PROVIDES TIMING AND MARK DATA.
.SBTL T0027
;*****
T0027: SCOPE
        MOV     #1000,SP    ;SETUP THE STACK POINTER
        JSR    PC,TORDER   ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
        00027             ;HERE LIES THE NUMBER OF THIS TEST
R0027: JSR    RS,BMOVE     ;SET CODE 55 IN MARK TRACK.
        MTK55
        MTK5
        6
        CLR     @TCCM
        MOV     #MAINT!UD!FWD!RNUM!DO,@TCCM
        MTCOD  MTK7,5
        JSR    RS,LATCOD   ;CALL LOAD MT CODES SUB.
        MTK7             ;ADDRESS OF MARK TRACK CODES.
        5                ;MARK TRACK CODE COUNT.
        TST     @TCST      ;ENDZ BIT SET?
        BPL     A0027      ;BR IF NOT SET.
        ERROR 36          ;MARK CODE 55 INTERPRETED AS END ZONE.

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 T0027

1429	005174	000404							
1430	005176	005777	174036						
1431	005202	100001							
1432	005204	104037							
1433	005206								
1434	005206	012706	001000						
1435	005212	000400							
1436									
1437									
1438									
1439									
1440	005214	000004							
1441	005216	012706	001000						
1442	005222	004737	011730						
1443	005226	000030							
1444	005230	004737	012136						
1445	005234	005274							
1446	005236	005077	173776						
1447	005242	012777	020103	173770					
1448	005250								
1449	005250	004537	012636						
1450	005254	033164							
1451	005256	000004							
1452	005260	105777	173754						
1453	005264	100402							
1454	005266	104040							
1455	005270	000401							
1456	005272	104003							
1457	005274								
1458	005274	012706	001000						
1459	005300	000400							
1460									
1461									
1462									
1463									
1464									
1465	005302	000004							
1466	005304	012706	001000						
1467	005310	004737	011730						
1468	005314	000031							
1469	005316	004737	012432						
1470	005322	004737	012136						
1471	005326	005472							
1472	005330	005077	173704						
1473	005334	012777	020103	173676					
1474	005342								
1475	005342	004537	012636						
1476	005346	033164							
1477	005350	000007							
1478	005352	005777	173662						
1479	005356	100002							
1480	005360	104041							
1481	005362	000440							
1482	005364	105777	173650						
1483	005370	100002							
1484	005372	104042							

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R0027: BR B0027
        TST @TCCM ; ERROR BIT SET?
        BPL B0027 ; BR IF NO ERROR.
        ERROR 37 ; ERROR BIT SET. EXAMINE TCST.

B0027: MOV #1000, SP ; RESTORE THE STACK POINTER
        BR T0030 ; GO ON TO THE NEXT TEST

; TEST THAT TC11 INTERRUPTS. RNUM COMMAND IS ISSUED. SUBROUTINE PROVIDES
; TIMING AND MARK. WHEN BLOCK IS FOUND INTERRUPT SHOULD OCCUR.
.SBTTL T0030
*****
T0030: SCOPE
        MOV #1000, SP ; SETUP THE STACK POINTER
        JSR PC, TORDER ; MAKE SURE TESTS ARE IN PROPER SEQUENCE
        00030 ; HERE LIES THE NUMBER OF THIS TEST
R0030: JSR PC, STTCV ; SET INTERRUPT VECTOR TO UE.
        00030
        CLR @TCCM
        MOV #MAINT!UO!FWD!IE!RNUM!DO, @TCCM
        MTCOD MTK7, 4
        JSR RS, LATCOD ; CALL LOAD MT CODES SUB.
        MTK7 ; ADDRESS OF MARK TRACK CODES.
        4 ; MARK TRACK CODE COUNT.
        TSTB @TCCM ; READY SET?
        BMI A0030 ; BR IF READY SET.
        ERROR 40 ; READY DID NOT SET.
A0030: BR 00030
        ERROR 3 ; READY FAILED TO INTERRUPT.
D0030: MOV #1000, SP ; RESTORE THE STACK POINTER
        BR T0031 ; GO ON TO THE NEXT TEST

; TEST THAT TC11 IS ABLE TO TRANSFER ONE WORD TO CORE STORAGE. SUBROUTINE
; PROVIDES TIMING AND MARK. AFTER BLOCK IS "FOUND" TEST SWITCHES TO
; RDATA COMMAND WITH WORD COUNT OF -1.
.SBTTL T0031
*****
T0031: SCOPE
        MOV #1000, SP ; SETUP THE STACK POINTER
        JSR PC, TORDER ; MAKE SURE TESTS ARE IN PROPER SEQUENCE
        00031 ; HERE LIES THE NUMBER OF THIS TEST
R0031: JSR PC, CLRBUF ; CLEAR READ BUFFER.
        JSR PC, STTCV ; SET INTERRUPT VECTOR TO VG.
        00031
        CLR @TCCM
        MOV #MAINT!UO!FWD!IE!RNUM!DO, @TCCM
        MTCOD MTK7, 7
        JSR RS, LATCOD ; CALL LOAD MT CODES SUB.
        MTK7 ; ADDRESS OF MARK TRACK CODES.
        7 ; MARK TRACK CODE COUNT.
        TST @TCCM ; ERROR BIT SET?
        BPL A0031 ; BR IF NO ERROR.
        ERROR 41 ; ERROR BIT SET. EXAMINE TCST.
A0031: BR F0031
        TSTB @TCCM ; READY BIT SET?
        BPL B0031 ; BR IF READY NOT SET.
        ERROR 42 ; READY SHOULD NOT BE SET.
  
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1485 005374 000433
1486 005376 022737 050505 036306 B0031: BR F0031
1487 005404 001405 BEQ #50505,RBUF ;SEE IF 1ST WORD IN RBUF IS 50505.
1488 005406 012737 050505 001162 MOV #50505,$REG0 ;BR IF WORD IS 50505.
1489 005414 104043 ERROR 43 ;GOOD DATA FOR PRINTOUT
1490 005416 000422 BR F0031 ;WORD IN RBUF IS NOT 50505. EXAMINE RBUF.
1491 005420 005777 173616 C0031: TST @TCWC ;TRANSFER MAY NOT HAVE OCCURRED.
1492 005424 001407 BEQ #0031 ;WORD COUNT 0?
1493 005426 017737 173610 001172 MOV @TCWC,$REG4 ;BR IF WORD COUNT IS 0.
1494 005434 005077 173522 CLR @SREG0 ;PREPARE ERONIOUS WORD COUNT FOR PRINTOUT
1495 005440 104044 ERROR 44 ;PREPARE GOOD WORD COUNT INFO FOR PRINTOUT
1496 005442 000410 BR F0031 ;WORD COUNT NOT 0.
1497 005444 022777 036310 173572 D0031: CMP #RBUF+2,@TCBA ;DID BUS ADDRESS INCREMENT CORRECTLY?
1498 005452 001404 BEQ F0031 ;BR IF TCBA IS CORRECT.
1499 005454 017737 173564 001172 MOV @TCBA,$REG4 ;TCBA DID NOT INCREMENT OR DID IT INCORRECTLY.
1500 005462 104045 ERROR 45
1501 005464 F0031:
1502 005464 012706 001000 MOV #1000,SP ;RESTORE THE STACK POINTER
1503 005470 000421 BR T0032 ;GO ON TO THE NEXT TEST
1504 005472 005777 173542 G0031: TST @TCCM ;HERE WHEN RNUM INTERRUPTS. ERROR BIT SET?
1505 005476 100004 BPL I0031 ;BR IF NO ERROR.
1506 005500 104041 ERROR 41 ;ERROR BIT SET. EXAMINE TCST.
1507
1508 005502 012706 001000 MOV #1000,SP ;RESTORE THE STACK POINTER
1509 005506 000412 BR T0032 ;GO ON TO THE NEXT TEST
1510 005510 012777 177777 173524 I0031: MOV #-1,@TCWC ;SET WORD COUNT TO -1.
1511 005516 012777 036306 173520 MOV #RBUF,@TCBA ;SET BUS ADDR TO RBUF.
1512 005524 112777 000005 173506 MOVB #RDATA!DO,@TCCM ;READ DATA COMMAND.
1513 005532 000002 RTI ;EXIT INTERRUPT.
1514 ;TEST THAT RDATA COMMAND WITH WORD COUNT SET TO -1 TRANSFERS ONLY ONE WORD.
1515 ;THAT READY IS SET WHEN THE ENTIRE 256 WORD BLOCK HAS BEEN PROCESSED, AND
1516 ;THAT NO PARITY ERROR OCCURS. TEST DONE UNDER MAINTENANCE MODE.
1517 .SBTTL T0032
1518 *****
1519 005534 000004
1520 005536 012706 001000 T0032: SCOPE
1521 005542 004737 011730 MOV #1000,SP ;SETUP THE STACK POINTER
1522 005546 000032 JSR PC,TORDER ;MAKE SURE TESTS ARE IN PRPOER SEQUENCE
1523 005550 004737 012432 R0032: JSR PC,CLRBUF ;HERE LIES THE NUMBER OF THIS TEST
1524 005554 004737 012136 JSR PC,STTCV ;CLEAR READ BUFFER.
1525 005560 005744 I0032 ;SET INTERRUPT VECTOR TO WI.
1526 005562 005077 173452 CLR @TCCM
1527 005566 012777 020103 173444 MOV #MAINT!UD!FWD!IE!RNUM!DO,@TCCM
1528 005574 MTCOD MTK7,267.
1529 005574 004537 012636 JSR RS,LATCOD ;CALL LOAD MT CODES SUB.
1530 005600 033164 MTK7 ;ADDRESS OF MARK TRACK CODES.
1531 005602 000413 267. ;MARK TRACK CODE COUNT.
1532 005604 005777 173430 TST @TCCM ;ERROR BIT SET?
1533 005610 100010 BPL B0032 ;BR IF NO ERROR.
1534 005612 032777 040000 173416 BIT #BIT14,@TCST ;WAS IT PARITY ERROR?
1535 005620 001402 BEQ A0032 ;BR IF NOT PARITY ERROR.
1536 005622 104046 ERROR 46 ;PARITY ERROR.
1537 005624 000444 BR H0032
1538 005626 104041 A0032: ERROR 41 ;ERROR BIT SET. NOT DUE TO PARITY ERROR.
1539 005630 000442 BR H0032
1540 005632 105777 173402 B0032: TSTB @TCCM ;READY BIT SET?

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1541 005636 100402      BMI      C0032      ; BR IF READY IS SET.
1542 005640 104047      ERROR 47          ; READY FAILED TO SET AFTER COMPLETION
1543 005642 000435      BR       H0032      ; OF RDATA COMMAND.
1544 005644 022737 050505 036306 C0032:  CMP     #50505,RBUF ; 1ST WORD EQUAL 50505?
1545 005652 001405      BEQ     D0032      ; BR IF WORD IS 50505.
1546 005654 012737 050505 001162      MOV     #50505,$REG0 ; GOOD DATA FOR PRINTOUT
1547 005662 104043      ERROR 43          ; 1ST WORD DID NOT TRANSFER TO RBUF CORRECTLY.
1548 005664 000424      BR       H0032
1549 005666 005737 036310      D0032:  TST     RBUF+2      ; RBUF+2 EQUAL 0?
1550 005672 001402      BEQ     F0032      ; BR IF RBUF+2 EQUAL 0.
1551 005674 104050      ERROR 50          ; RBUF+2 NOT 0. NO DATA SHOULD HAVE
1552 005676 000417      BR       H0032      ; TRANSFERRED TO IT.
1553 005700 005777 173336      F0032:  TST     @TCWC      ; WORD COUNT 0?
1554 005704 001407      BEQ     G0032      ; BR IF WORD COUNT IS 0.
1555 005706 017737 173330 001172      MOV     @TCWC,$REG4 ; PREPARE ERONIOUS WORD COUNT FOR PRINTOUT
1556 005714 005077 173242      CLR     @SREG0      ; PREPARE GOOD WORD COUNT INFO FOR PRINTOUT
1557 005720 104044      ERROR 44          ; WORD COUNT NOT 0.
1558 005722 000405      BR       H0032
1559 005724 022777 036310 173312 G0032:  CMP     #RBUF+2,@TCBA ; IS BUS ADDR CORRECT?
1560 005732 001401      BEQ     H0032      ; BR IF TCBA OK.
1561 005734 104045      ERROR 45          ; TCBA ADDR INCORRECT. SHOULD CONTAIN RBUF+2.
1562 005736      H0032:
1563 005736 012706 001000      MOV     #1000,SP    ; RESTORE THE STACK POINTER
1564 005742 000421      BR       T0033      ; GO ON TO THE NEXT TEST
1565 005744 005777 173270      I0032:  TST     @TC      ; HERE WHEN RNUM INTERRUPTS. ERROR?
1566 005750 100004      BPL     K0032      ; BR IF NO ERROR.
1567 005752 104041      ERROR 41          ; ERROR BIT SET. EXAMINE TCST.
1568
1569 005754 012706 001000      MOV     #1000,SP    ; RESTORE THE STACK POINTER
1570 005760 000412      BR       T0033      ; GO ON TO THE NEXT TEST
1571 005762 012777 177777 173252 K0032:  MOV     #-1,@TCWC   ; SET WORD COUNT TO -1.
1572 005770 012777 036306 173246      MOV     #RBUF,@TCBA ; SET BUS ADDR TO RBUF.
1573 005776 112777 000005 173234      MOVB   #RDATA!DO,@TCCH ; READ DATA COMMAND.
1574 006004 000002      RTI          ; EXIT INTERRUPT.
1575 ; TEST THAT TC11 IS ABLE TO DETECT INCORRECT PARITY. RDATA COMMAND IS ISSUED.
1576 ; TCWC=-1. BLOCK TO BE READ CONTAINS BAD CHECKSUM. TEST DONE IN MAINT. MODE.
1577 ; SBTTL T0033
1578 ; *****
1579 006006 000004      T0033:  SCOPE
1580 006010 012706 001000      MOV     #1000,SP    ; SETUP THE STACK POINTER
1581 006014 004737 011730      JSR     PC,TORDER   ; MAKE SURE TESTS ARE IN PRPOER SEQUENCE
1582 006020 000033      00033      ; HERE LIES THE NUMBER OF THIS TEST
1583 006022 004737 013114      R0033:  JSR     PC,MBCKSM    ; BAD CHECKSUM TO FCKSM.
1584 006026 004737 012432      JSR     PC,CLRBUF   ; CLEAR READ BUFFER.
1585 006032 004737 012136      JSR     PC,STTCV    ; SET INTERRUPT VECTOR TO XE.
1586 006036 006154      D0033
1587 006040 005077 173174      CLR     @TCCH
1588 006044 012777 020103 173166      MOV     #MAINT!UO!FWD!IE!RNUM!DO,@TCCH
1589 006052      MTCOD
1590 006052 004537 012636      JSR     R5,LATCOD   ; CALL LOAD MT CODES SUB.
1591 006056 033164      MTK7      ; ADDRESS OF MARK TRACK CODES.
1592 006060 000413      267.      ; MARK TRACK CODE COUNT.
1593 006062 032777 040000 173146      BIT     #BIT14,@TCST ; PARITY ERROR SET?
1594 006070 001005      BNE     A0033      ; BR IF PARITY ERROR SET.
1595 006072 017737 173144 001162      MOV     @TCWC,$RE ;D
1596 006100 104052      ERROR 52          ; PARITY ERROR NOT DETECTED.(BIT NOT SET).

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M03

MAINDEC-11-DZTCB-D  
DZTCB0.P11

TC11 TEST #2  
18-FEB-77 10:59

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T0033

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1597 006102 000421
1598 006104 005777 173130
1599 006110 100405
1600 006112 017737 173124 001162
1601 006120 104053
1602 006122 000411
1603 006124 005077 173110
1604 006130 005777 173104
1605 006134 100004
1606 006136 017737 173100 001162
1607 006144 104054
1608 006146
1609 006146 012706 001000
1610 006152 000421
1611 006154 005777 173060
1612 006160 100004
1613 006162 104041
1614
1615 006164 012706 001000
1616 006170 000412
1617 006172 012777 177777 173042
1618 006200 012777 036306 173036
1619 006206 112777 000005 173024
1620 006214 000002
1621
1622
1623
1624
1625 006216 000004
1626 006220 012706 001000
1627 006224 004737 011730
1628 006230 000034
1629 006232 004737 012432
1630 006236 004737 012136
1631 006242 006360
1632 006244 005077 172770
1633 006250 012777 020103 172762
1634 006256
1635 006256 004537 012636
1636 006262 033164
1637 006264 000413
1638 006266 005777 172746
1639 006272 100002
1640 006274 104041
1641 006276 000425
1642 006300 005777 172736
1643 006304 001407
1644 006306 017737 172730 001172
1645 006314 005077 172642
1646 006320 104044
1647 006322 000413
1648 006324 022777 037306 172712
1649 006332 001402
1650 006334 104051
1651 006336 000405
1652 006340 004537 013130

A0033: BR C0033
TST @TCCM ;ERROR BIT SET?
BMI B0033 ;BR IF ERROR BIT SET.
MOV @TWC, $REG0
ERROR 53 ;PARITY ERROR DID NOT SET ERROR BIT.

B0033: BR C0033
CLR @TCCM ;CLEAR COMMAND REGISTER.
TST @TCCM ;ERROR BIT CLEAR?
BPL C0033 ;BR IF ERROR BIT IS CLEAR.
MOV @TWC, $REG0
ERROR 54 ;CLEARING TCCM FAILED TO CLEAR PARITY ERROR.

C0033: MOV #1000, SP ;RESTORE THE STACK POINTER
BR T0034 ;GO ON TO THE NEXT TEST
D0033: TST @TCCM ;HERE WHEN RNUM INTERRUPTS. ERROR?
BPL G0033 ;BR IF NO ERROR.
ERROR 41 ;ERROR BIT SET. EXAMINE TCST.

MOV #1000, SP ;RESTORE THE STACK POINTER
BR T0034 ;GO ON TO THE NEXT TEST
G0033: MOV #-1, @TWC ;-1 TO WORD COUNT.
MOV @RBUF, @TCBA ;SET BUS ADDR TO RBUF.
MOVB @RDATA!DO, @TCCM ;RDATA COR. AND.
RTI ;EXIT INTERRUPT.
;READ 256 WORDS WITH RDATA COMMAND UNDER MAINTENANCE MODE. ALL DATA SHOULD
;TRANSFER CORRECTLY. NO CONTROL ERRORS SHOULD OCCUR.
.SBTL T0034
*****
T0034: SCOPE
MOV #1000, SP ;SETUP THE STACK POINTER
JSR PC, TORDER ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
00034 ;HERE LIES THE NUMBER OF THIS TEST
R0034: JSR PC, CLRBUF ;CLEAR READ BUFFER.
JSR PC, STICV ;SET INTERRUPT VECTOR TO YF.
F0034
CLR @TCCM
MOV @MAINT!UD!FWD!IE!RNUM!DO, @TCCM
MTCOD MTK7, 267.
JSR R5, LATCOD ;CALL LOAD MT CODES SUB.
MTK7 ;ADDRESS OF MARK TRACK CODES.
267. ;MARK TRACK CODE COUNT.
TST @TCCM ;ERROR BIT SET?
BPL A0034 ;BR IF NO ERROR.
ERROR 41 ;ERROR BIT SET. EXAMINE TCST.

A0034: BR D0034
TST @TWC ;WORD COUNT 0?
BEQ B0034 ;BR IF WORD COUNT IS 0.
MOV @TWC, $REG4 ;PREPARE ERONIOUS WORD COUNT FOR PRINTOUT
CLR @SREG0 ;PREPARE GOOD WORD COUNT INFO FOR PRINTOUT
ERROR 44 ;WORD COUNT NOT 0.

B0034: BR D0034
CMP @RBUF+512., @TCBA ;BUS ADDR CORRECT?
BEQ C0034 ;BR IF TCBA OK.
ERROR 51 ;TCBA INCORRECT. SHOULD BE EQUAL TO
BR D0034 ;RBUF+512.
C0034: JSR R5, CKDAT ;COMPARE 256 WORDS STARTING AT RBUF.

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1653 006344 001276          SBDAT1          ;REPORT ANY ERRORS.
1654 006346 036306          RBUF
1655 006350 000400          256.
1656 006352
1657 006352 012706 001000    D0034:  MOV      #1000,SP      ;RESTORE THE STACK POINTER
1658 006356 000421          BR          T0035        ;GO ON TO THE NEXT TEST
1659 006360 005777 172654    F0034:  TST      @TCM         ;HERE WHEN RNUM INTERRUPTS. ERROR?
1660 006364 100004          BPL        H0034        ;BR IF NO ERROR.
1661 006366 104041          ERROR 41          ;ERROR BIT SET. EXAMINE TCST.
1662
1663 006370 012706 001000    MOV      #1000,SP      ;RESTORE THE STACK POINTER
1664 006374 000412          BR          T0035        ;GO ON TO THE NEXT TEST
1665 006376 012777 177400 172636  H0034:  MOV      #-256,@TCWC    ;-256 TO WORD COUNT.
1666 006404 012777 036306 172632  MOV      #RBUF,@TCBA   ;SET BUS ADDR TO RBUF.
1667 006412 112777 000005 172620  MOVB     @RDATA!DO,@TCM ;READ DATA COMMAND.
1668 006420 000002          RTI                ;EXIT INTERRUPT.
1669
1670          ;READ 2 DATA BLOCKS (512 WORDS) WITH RDATA COMMAND UNDER MAINTENANCE MODE.
1671          ;ALL DATA SHOULD TRANSFER CORRECTLY. NO ERRORS SHOULD OCCUR.
1672          .SBTTL T0035
1673          *****
1673 006422 000004          T0035:  SCOPE
1674 006424 012706 001000    MOV      #1000,SP      ;SETUP THE STACK POINTER
1675 006430 004737 011730    JSR      PC,TORDER     ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
1676 006434 000035          00035             ;HERE LIES THE NUMBER OF THIS TEST
1677 006436 004737 012432    R0035:  JSR      PC,CLRBUF     ;CLEAR READ BUFFER.
1678 006442 004737 012136    JSR      PC,STTCV      ;SET INTERRUPT VECTOR TOZF.
1679 006446 006564          F0035
1680 006450 005077 172564    CLR      @TCM
1681 006454 012777 020103 172556  MOV      #MAINT!UO!FWD!IE!RNUM!DO,@TCM
1682 006462          MTCOD
1683 006462 004537 012636    JSR      MTK7,534.     ;CALL LOAD MT CODES SUB.
1684 006466 033164          MTK7             ;ADDRESS OF MARK TRACK CODES.
1685 006470 001026          534.            ;MARK TRACK CODE COUNT.
1686 006472 005777 172542    TST      @TCM         ;ERROR BIT SET?
1687 006476 100002          BPL        A0035      ;BR IF NO ERROR.
1688 006500 104041          ERROR 41        ;ERROR BIT SET EXAMINE TCST.
1689 006502 000425          BR          D0035
1690 006504 005777 172532    A0035:  TST      @TCWC        ;WORD COUNT 0?
1691 006510 001407          BEQ        B0035      ;BR IF WORD COUNT IS 0.
1692 006512 017737 172524 001172  MOV      @TCWC,@RREG4 ;PREPARE ERONIOUS WORD COUNT FOR PRINTOUT
1693 006520 005077 172436    CLR      @RREG0 ;PREPARE GOOD WORD COUNT INFO FOR PRINTOUT
1694 006524 104044          ERROR 44        ;WORD COUNT NOT 0.
1695 006526 000413          BR          D0035
1696 006530 022777 040306 172506  B0035:  CMP      #RBUF+1024.,@TCBA ;TCBA CORRECT?
1697 006536 001402          BEQ        C0035      ;BR IF TCBA IS OK.
1698 006540 104045          ERROR 45        ;TCBA INCORRECT. SHOULD BE RBUF+1024.
1699 006542 000405          BR          D0035
1700 006544 004537 013130    C0035:  JSR      RS,CKDAT     ;COMPARE 512 WORDS STARTING AT RBUF.
1701 006550 001276          SBDAT1          ;REPORT ANY ERRORS.
1702 006552 036306          RBUF
1703 006554 001000          512.
1704 006556
1705 006556 012706 001000    D0035:  MOV      #1000,SP      ;RESTORE THE STACK POINTER
1706 006562 000421          BR          T0036      ;GO ON TO THE NEXT TEST
1707 006564 005777 172450    F0035:  TST      @TCM         ;HERE WHEN RNUM INTERRUPTS. ERROR?
1708 006570 100004          BPL        H0035      ;BR IF NO ERROR.

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1709 006572 104041          ERROR 41          ;ERROR BIT SET. EXAMINE TCST.
1710
1711 006574 012706 001000    MOV      #1000,SP      ;RESTORE THE STACK POINTER
1712 006600 000412          BR        T0036       ;GO ON TO THE NEXT TEST
1713 006602 012777 177000 172432 H0035:  MOV      #-512,@TCWC   ; -512 TO WORD COUNT.
1714 006610 012777 036306 172426    MOV      #RBUF,@TCBA  ;SET BUS ADDR TO RBUF.
1715 006616 112777 000005 172414    MOVB    #RDATA!DO,@TCCH ;READ DATA COMMAND.
1716 006624 000002          RTI                 ;EXIT INTERRUPT.
1717          ;READ 1.5 BLOCKS (384 WORDS) WITH RDATA COMMAND UNDER MAINTENANCE MODE.
1718          ;ALL DATA SHOULD TRANSFER CORRECTLY. NO ERRORS SHOULD OCCUR.
1719          .SBTTL T0036
1720          ;*****
1721 006626 000004          T0036:  SCOPE
1722 006630 012706 001000    MOV      #1000,SP      ;SETUP THE STACK POINTER
1723 006634 004737 011730    JSR     PC,TOADR       ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
1724 006640 000036          00036    ;HERE LIES THE NUMBER OF THIS TEST
1725 006642 004737 012432    R0036:  JSR     PC,CLRBUF      ;CLEAR READ BUFFER.
1726 006646 004737 012136    JSR     PC,STTCV      ;SET INTERRUPT VECTOR TO AIF.
1727 006652 006766          F0036
1728 006654 005077 172360    CLR     @TCCH
1729 006660 012777 020103 172352    MOV      #MAINT!UD!FWD!IE!RNUM!DO,@TCCH
1730 006666          MTC00  MTK7,534.
1731 006672 004537 012636    JSR     RS,LATC00     ;CALL LOAD MT CODES SUB.
1732 006674 001026          MTK7     ;ADDRESS OF MARK TRACK CODES.
1733 006676 005777 172336    534.     ;MARK TRACK CODE COUNT.
1734 006702 100002          TST     @TCCH        ;ERROR BIT SET?
1735 006704 104041          BPL     A0036        ;BR IF NO ERROR.
1736 006706 000424          ERROR 41          ;ERROR BIT SET. EXAMINE TCST.
1737 006710 005777 172326          BR      D0036
1738 006714 001407          A0036:  TST     @TCWC        ;WORD COUNT 0?
1739 006716 017737 172320 001172    BEQ     B0036        ;BR IF WORD COUNT 0.
1740 006724 005077 172232          MOV     @TCWC,@REG4  ;PREPARE ERONIOUS WORD COUNT FOR PRINTOUT
1741 006730 104044          CLR     @SREG0       ;PREPARE GOOD WORD COUNT INFO FOR PRINTOUT
1742 006732 000412          ERROR 44          ;WORD COUNT NOT 0.
1743 006734 022777 037706 172302    B0036:  CMP     #RBUF+768.,@TCBA ;TCBA CORRECT?
1744 006742 001401          BEQ     C0036        ;BR IF TCBA OK.
1745 006744 104045          ERROR 45          ;TCBA INCORRECT. SHOULD BE RBUF+768.
1746 006746 004537 013130          C0036:  JSR     RS,CKDAT     ;COMPARE 384 WORDS STARTING AT RBUF.
1747 006752 001276          SBDAT1 ;REPORT ANY ERRORS.
1748 006754 036306          RBUF
1749 006756 000600          384.
1750
1751 006760          D0036:
1752 006762 012706 001000    MOV      #1000,SP      ;RESTORE THE STACK POINTER
1753 006764 000421          BR      T0037       ;GO ON TO THE NEXT TEST
1754 006766 005777 172246          F0036:  TST     @TCCH        ;HERE WHEN RNUM INTERRUPTS. ERROR?
1755 006772 100004          BPL     H0036        ;BR IF NO ERROR.
1756 006774 104041          ERROR 41          ;ERROR BIT SET. EXAMINE TCST.
1757
1758 006776 012706 001000    MOV      #1000,SP      ;RESTORE THE STACK POINTER
1759 007002 000412          BR      T0037       ;GO ON TO THE NEXT TEST
1760 007004 012777 177200 172230    H0036:  MOV      #-384,@TCWC   ; -384 TO WORD COUNT.
1761 007012 012777 036306 172224    MOV     #RBUF,@TCBA  ;SET BUS ADDR TO RBUF.
1762 007020 112777 000005 172212    MOVB    #RDATA!DO,@TCCH ;READ DATA COMMAND.
1763 007026 000002          RTI                 ;EXIT INTERRUPT.
1764          ;COMPLEMENT OBVERSE READ TEST. READ ONE BLOCK (256 WORDS) WITH RDATA IN REVERSE.

```

```

1765
1766
1767
1768 007030 000004
1769 007032 012706 001000
1770 007036 004737 011730
1771 007042 000037
1772 007044 004737 012432
1773 007050 004737 012136
1774 007054 007132
1775 007056 005077 172156
1776 007062 012777 024103 172150
1777 007070
1778 007070 004537 012636
1779 007074 033164
1780 007076 000413
1781 007100 005777 172134
1782 007104 100002
1783 007106 104041
1784 007110 000405
1785 007112 004537 013130
1786 007116 001302
1787 007120 036306
1788 007122 000400
1789 007124
1790 007124 012706 001000
1791 007130 000421
1792 007132 005777 172102
1793 007136 100004
1794 007140 104041
1795
1796 007142 012706 001000
1797 007146 000412
1798 007150 012777 177400 172064
1799 007156 012777 036306 172060
1800 007164 112777 000005 172046
1801 007172 000002
1802
1803
1804
1805 007174 000004
1806 007176 012706 001000
1807 007202 004737 011730
1808 007206 000040
1809 007210 005077 172024
1810 007214 012777 177776 172020
1811 007222 012777 036306 172014
1812 007230 012777 020003 172002
1813 007236
1814 007236 004537 012636
1815 007242 033164
1816 007244 000005
1817 007246 005777 171766
1818 007252 100002
1819 007254 104041
1820 007256 000506

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; ALL DATA SHOULD COMPLEMENT OBVERSE CORRECTLY. NO CONTROL ERRORS SHOULD OCCUR.

.SBTTL T0037

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T0037: SCOPE
MOV #1000,SP ; SETUP THE STACK POINTER
JSR PC,TORDER ; MAKE SURE TESTS ARE IN PROPER SEQUENCE
00037 ; HERE LIES THE NUMBER OF THIS TEST
R0037: JSR PC,CLRBUF ; CLEAR READ BUFFER
JSR PC,STTCV ; SET INTERRUPT VECTOR TO BID
C0037
CLR @TCCM
MOV @MAINT!LD!REV!IE!RNUM!DO,@TCCM
MTCOD MTK7,267.
JSR RS,LATCOD ; CALL LOAD MT CODES SUB.
MTK7 ; ADDRESS OF MARK TRACK CODES.
267. ; MARK TRACK CODE COUNT.
TST @TCCM ; ERROR BIT SET?
BPL A0037 ; BR IF NO ERROR.
ERROR 41 ; ERROR BIT SET. EXAMINE TCST.
BR B0037
A0037: JSR RS,CKDAT ; COMPARE 256 WORDS STARTING AT RBUF.
SBOAT2 ; REPORT ANY ERRORS.
RBUF 256.
B0037:
MOV #1000,SP ; RESTORE THE STACK POINTER
BR T0040 ; GO ON TO THE NEXT TEST
C0037: TST @TCCM ; HERE WHEN RNUM INTERRUPTS. ERROR.
BPL F0037 ; BR IF NO ERROR.
ERROR 41 ; ERROR BIT SET. EXAMINE TCST.
MOV #1000,SP ; RESTORE THE STACK POINTER
BR T0040 ; GO ON TO THE NEXT TEST
F0037: MOV #-256,@TCCW ; -256 TO AND COUNT.
MOV @RBUF,@TCBA ; ADDR OF RBUF TO BUS ADDRESS.
MOVB @RDATA!DO,@TCCM ; READ DATA COMMAND.
RTI ; EXIT INTERRUPT
; CHECK FOR CORRECT OPERATION OF BLOCK MISS ERROR.

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.SBTTL T0040

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T0040: SCOPE
MOV #1000,SP ; SETUP THE STACK POINTER
JSR PC,TORDER ; MAKE SURE TESTS ARE IN PROPER SEQUENCE
00040 ; HERE LIES THE NUMBER OF THIS TEST
R0040: CLR @TCCM
MOV #-2,@TCCW ; -2 TO WORD COUNT.
MOV @RBUF,@TCBA ; RBUF ADDR TO TCBA.
MOV @MAINT!LD!FWD!RNUM!DO,@TCCM
MTCOD MTK7,5
JSR RS,LATCOD ; CALL LOAD MT CODES SUB.
MTK7 ; ADDRESS OF MARK TRACK CODES.
5 ; MARK TRACK CODE COUNT.
TST @TCCM ; ERROR BIT SET?
BPL A0040 ; BR IF NO ERROR.
R0040A: ERROR 41 ; ERROR BIT SET EXAMINE TCST.
BR F0040

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```

1821 007260 112777 000005 171752 R0040: MOVB #RDATA!DO,@TCCH ;ISSUE RDATA COMMAND.
1822 007266 MTCOD MTK7A,2
1823 007266 004537 012636 JSR RS,LMTCOD ;CALL LOAD MT CODES SUB.
1824 007272 033222 MTK7A ;ADDRESS OF MARK TRACK CODES.
1825 007274 000002 2 ;MARK TRACK CODE COUNT.
1826 007276 032777 002000 171732 BIT #BIT10,@TCST ;BLOCK MISS ERROR SET?
1827 007304 001405 BEQ R0040 ;BR IF NO BLOCK MISS. OK.
1828 007306 017737 171730 001162 MOV @TCWC,$REGO ;MAKE WORD COUNT INFO PRINTABLE
1829 007314 104055 ERROR 55 ;BLOCK MISS SET WHEN RDATA ISSUED JUST
1830 007316 000466 BR F0040 ;BEFORE REV CHECK MARK. SHOULDN'T HAVE.
1831 007320 005077 171714 B0040: CLR @TCCH
1832 007324 012777 177776 171710 MOV #-2,@TCWC ;-2 TO WORD COUNT.
1833 007332 012777 036306 171704 MOV #RBUF,@TCBA ;RBUF ADDR TO TCBA.
1834 007340 012777 020003 171672 MOV #MAINT!UO!FWD!RNUM!DO,@TCCH
1835 007346 MTCOD MTK7,6
1836 007346 004537 012636 JSR RS,LMTCOD ;CALL LOAD MT CODES SUB.
1837 007352 033164 MTK7 ;ADDRESS OF MARK TRACK CODES.
1838 007354 003006 6 ;MARK TRACK CODE COUNT.
1839 007356 005777 171656 TST @TCCH ;ERROR BIT SET?
1840 007362 100734 BMI R0040A ;BR IF ERROR BIT SET?
1841 007364 112777 000005 171646 MOVB #RDATA!DO,@TCCH ;ISSUE RDATA COMMAND.
1842 007372 MTCOD MTK7B,2
1843 007372 004537 012636 JSR RS,LMTCOD ;CALL LOAD MT CODES SUB.
1844 007376 033230 MTK7B ;ADDRESS OF MARK TRACK CODES.
1845 007400 000002 2 ;MARK TRACK CODE COUNT.
1846 007402 032777 002000 171626 BIT #BIT10,@TCST ;BLOCK MISS ERROR SET?
1847 007410 001005 BNE R0040 ;BR IF BLOCK MISS.
1848 007412 017737 171624 001162 MOV @TCWC,$REGO ;MAKE WORD COUNT INFO PRINTABLE
1849 007420 104056 ERROR 56 ;BLOCK MISS FAILED TO SET WHEN RDATA ISSUED
1850 007422 000424 BR F0040 ;RIGHT AFTER REV CHECK MARK. IT SHOULD HAVE.
1851 007424 005777 171610 C0040: TST @TCCH ;ERROR BIT SET?
1852 007430 100405 BMI R0040 ;BR IF ERROR BIT SET.
1853 007432 017737 171604 001162 MOV @TCWC,$REGO ;MAKE WORD COUNT INFO PRINTABLE
1854 007440 104057 ERROR 57 ;BLOCK MISS FAILED TO SET ERROR BIT.
1855 007442 000414 BR F0040
1856 007444 005077 171570 D0040: CLR @TCCH ;0 TO ERROR BIT.
1857 007450 032777 002000 171562 BIT #BIT10,@TCCH ;BLOCK MISS CLEARED?
1858 007456 001406 BEQ F0040 ;BR IF BLOCK MISS CLEARED.
1859 007460 017737 171556 001162 MOV @TCWC,$REGO ;MAKE WORD COUNT INFO PRINTABLE
1860 007466 104060 ERROR 60 ;0 TO ERROR FAILED TO CLEAR BLOCK MISS.
1861 007470 004737 012162 JSR PC,SRSETT
1862 007474 F0040:
1863 007474 012706 0C1000 MOV #1000,SP ;RESTORE THE STACK POINTER
1864 007500 000400 BR T0041 ;GO ON TO THE NEXT TEST
1865 ;READ ALL TEST (RALL)
1866 ;AFTER BLOCK IS FOUND, SWITCH TO RALL. READ 258 WORDS. 1ST WORD READ SHOULD BE
1867 ;THE REVERSE CHECKSUM (SHOULD BE 0). LAST WORD READ SHOULD BE THE FORWARD
1868 ;CHECKSUM (SHOULD BE 770000). ALL OTHER WORDS SHOULD BE DATA.
1869 .SBTTL T0041
1870 *****
1871 007502 000004 T0041: SCOPE
1872 007504 012706 001000 MOV #1000,SP ;SETUP THE STACK POINTER
1873 007510 004737 011730 JSR PC,TORDER ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
1874 007514 000041 00041 ;HERE LIES THE NUMBER OF THIS TEST
1875 007516 004737 012432 R0041: JSR PC,CLRBUF ;CLEAR READ BUFFER.
1876 007522 004737 012136 JSR PC,STTCV ;SET INTERRUPT VECTOR TO EIF.

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E04

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1877	007526	007716				F0041			
1878	007530	005077	171504			CLR	@TCCM		
1879	007534	012777	020103	171476		MOV	#MAINT!UO!FWD!IE!RNUM!DO,@TCCM		
1880	007542					MTC00	MTK7,267.		
1881	007542	004537	012636			JSR	RS,LATC00		: CALL LOAD MT CODES SUB.
1882	007546	033164				MTK7			: ADDRESS OF MARK TRACK CODES.
1883	007550	000413				267.			: MARK TRACK CODE COUNT.
1884	007552	005777	171462		R0041A:	TST	@TCCM		: ERROR BIT SET?
1885	007556	100002				BPL	R0041B		: BR IF NO ERROR.
1886	007560	104041				ERROR 41			: ERROR BIT SET. EXAMINE TCST.
1887	007562	000461				BR	G0041		
1888	007564	017724	171456		R0041B:	MOV	@TCOT,(4)+		: SAVE DATA IN READ BUFFER.
1889	007570	005337	001274			DEC	CTRA		: 258 WORDS READ?
1890	007574	001401				BEQ	A0041		: BR IF 258 WORDS READ.
1891	007576	000002				RTI			: NOT DONE YET. EXIT INTERRUPT.
1892	007600	005737	036306		A0041:	TST	RBUF		: 1ST WORD IN RBUF EQUAL 0?
1893	007604	001416				BEQ	D0041		: BR IF 1ST WORD IS 0.
1894	007606	022737	055555	036306		CMP	#5555,RBUF		: 1ST WORD EQUAL 5555?
1895	007614	001002				BNE	B0041		: BR IF NOT 5555.
1896	007616	104043				ERROR 43			: 5555. 1ST WORD READ WITH RALL WAS
1897	007620	000442				BR	G0041		: REV GUARD INSTEAD OF REV CHECKSUM.
1898	007622	022737	066666	036306	B0041:	CMP	#66666,RBUF		: 1ST WORD EQUAL 66666?
1899	007630	001002				BNE	C0041		: BR IF NOT 66666.
1900	007632	104043				ERROR 43			: 66666. 1ST WORD READ WITH RALL WAS
1901	007634	000434				BR	G0041		: REV LOCK INSTEAD OF REV CHECKSUM.
1902	007636	104043			C0041:	ERROR 43			: 1ST WORD READ WITH RALL WAS NOT
1903	007640	000432				BR	G0041		: REV CHECKSUM. EXAMINE RBUF (1ST WORD).
1904	007642	004537	013130		D0041:	JSR	RS,CKDAT		
1905	007646	001276				SBDAT1			
1906	007650	036310				RBUF+2			
1907	007652	000400				256.			
1908	007654	022737	170000	037310		CMP	#170000,RBUF+514.;FWD CHKSUM EQUAL 170000? 1ST WORD READ.		
1909	007662	001402				BEQ	D0041A		
1910	007664	104061				ERROR 61			: LAST WORD READ SHOULD HAVE BEEN THE FWD CHECKSUM.
1911	007666	000417				BR	G0041		: IN CORE IT SHOULD BE 170000.
1912	007670	005777	171346		D0041A:	TST	@TCWC		: WORD COUNT STILL 0?
1913	007674	001402				BEQ	D0041B		
1914	007676	104062				ERROR 62			: TCWC (WORD COUNT) WAS MODIFIED DURING
1915	007700	000412				BR	G0041		: RALL. SHOULDN'T HAVE.
1916	007702	022777	036306	171334	D0041B:	CMP	#RBUF,@TCBA		: BUS ADDRESS STILL EQUAL #RBUF?
1917	007710	001406				BEQ	G0041		
1918	007712	104063				ERROR 63			: TCBA (BUS ADDRESS) MODIFIED DURING
1919	007714	000404				BR	G0041		: RALL. SHOULDN'T HAVE.
1920	007716	005777	171316		F0041:	TST	@TCCM		: HERE WHEN RNUM INTERRUPTS. ERROR!
1921	007722	100004				BPL	I0041		: BR IF NO ERROR.
1922	007724	104041				ERROR 41			: ERROR BIT SET. EXAMINE TCST.
1923	007726				G0041:				
1924	007726	012706	001000			MOV	#1000,SP		: RESTORE THE STACK POINTER
1925	007732	000421				BR	T0042		: GO ON TO THE NEXT TEST
1926	007734	012737	000402	001274	I0041:	MOV	#258,CTRA		: NUMBER OF WORDS TO READ TO CTRA.
1927	007742	012704	036306			MOV	#RBUF,R4		: ADDR TO STORE DATA TO R4.
1928	007746	005077	171270			CLR	@TCWC		: ZERO WORD COUNT.
1929	007752	012777	036306	171264		MOV	#RBUF,@TCBA		: SET BUS ADDRESS TO RBUF.
1930	007760	004737	012136			JSR	PC,STCV		: SET INTERRUPT VECTOR TO E1AA.
1931	007764	007552				R0041A			
1932	007766	112777	000107	171244		MOVB	#RALL!IE!DO,@TCCM		: RALL COMMAND.

1933 007774 000002  
1934  
1935  
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1940 007776 000004  
1941 010000 012706 001000  
1942 010004 004737 011730  
1943 010010 000042  
1944 010012 004737 012136  
1945 010016 010120  
1946 010020 005077 171214  
1947 010024 012777 020103 171206  
1948 010032  
1949 010032 004537 012636  
1950 010036 033164  
1951 010040 000007  
1952 010042 032777 001000 171166  
1953 010050 001002  
1954 010052 104064  
1955 010054 000416  
1956 010056 005777 171156  
1957 010062 100402  
1958 010064 104065  
1959 010066 000411  
1960 010070 005077 171144  
1961 010074 032777 001000 171134  
1962 010102 001403  
1963 010104 104066  
1964 010106 004737 012162  
1965 010112  
1966 010112 012706 001000  
1967 010116 000422  
1968 010120 005777 171114  
1969 010124 100004  
1970 010126 104041  
1971  
1972 010130 012706 001000  
1973 010134 000413  
1974 010136 004737 012136  
1975 010142 010154  
1976 010144 112777 000107 171066  
1977 010152 000002  
1978 010154 112777 000007 171056  
1979 010162 000002  
1980  
1981  
1982  
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1984  
1985  
1986  
1987  
1988 010164 000004

```
RTI ;EXIT INTERRUPT.
;DATA MISS TEST. TEST THAT DATA MISS ERROR SETS WHEN DATA REGISTER (TCDT) IS
;NOT REFERENCED UNDER RALL COMMAND, BEFORE THE NEXT DATA WORD IS LOADED INTO
;THE DATA REGISTER. (READY BIT IS CLEARED WHEN IN RALL BY REFERENCING
;THE DATA REGISTER (TCDT).
.SBTL T0042
*****
T0042: SCOPE
MOV #1000,SP ;SETUP THE STACK POINTER
JSR PC,TORDER ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
00042 ;HERE LIES THE NUMBER OF THIS TEST
R0042: JSR PC,STTCV ;SET INTERRUPT VECTOR TO FIE.
D0042
CLR @TCCM
MOV #MAINT!UO!FWD!IE!RNUM!DO,@TCCM
MTCO0 MTK7,7
JSR RS,LATCOO ;CALL LOAD MT CODES SUB.
MTK7 ;ADDRESS OF MARK TRACK CODES.
7 ;MARK TRACK CODE COUNT.
BIT #BIT9,@TCST ;DATA MISS ERROR SET?
BNE R0042 ;BR IF DATA MISS IS SET.
ERROR 64 ;DATA MISS FAILED TO SET.
R0042: BR C0042
TST @TCCM ;ERROR BIT SET?
BMI B0042 ;BR IF ERROR BIT SET.
ERROR 65 ;DATA MISS FAILED TO SET ERROR BIT.
B7 C0042
B0042: CLR @TCCM ;0 TO ERROR BIT.
BIT #BIT9,@TCST ;DATA MISS CLEARED?
BEQ C0042 ;BR IF DATA MISS IS CLEAR.
ERROR 66 ;0 TO ERROR FAILED TO CLEAR DATA MISS.
JSR PC,SRSETT
C0042: MOV #1000,SP ;RESTORE THE STACK POINTER
BR T0043 ;GO ON TO THE NEXT TEST
D0042: TST @TCCM ;HERE WHEN RNUM INTERRUPTS. ERROR?
BPL G0042 ;BR IF NO ERROR.
ERROR 41 ;ERROR BIT SET. EXAMINE TCST.
MOV #1000,SP ;RESTORE THE STACK POINTER
BR T0043 ;GO ON TO THE NEXT TEST
G0042: JSR PC,STTCV ;SET INTERRUPT VECTOR TO F1H.
H0042
MOV #RALL!IE!DO,@TCCM ;ISSUE RALL. IE SET.
RTI ;EXIT INTERRUPT.
H0042: MOV #RALL!DO,@TCCM ;HERE WHEN RALL INTERRUPTS. DISABLE INTERRUPTS,
;DO NOT READ TCDT, EXIT INTERRUPT.
;WRITE DATA TEST. AFTER BLOCK NUMBER IS "FOUND" ISSUE WDATA COMMAND
;UNDER MAINTENANCE MODE, WORD COUNT = -256, TCBA = RBUF. AFTER
;EACH MARK TRACK CODE IS PASSED, THE DATA IN THE DATA REGISTER IS SAVED.
;WHEN THE OPERATION IS COMPLETED, A COMPARE OF WRITE DATA AND THE DATA
;REGISTER DATA SAVED IS MADE TO SEE IF THEY MATCH. WORD COUNT AND TCBA
;ARE ALSO CHECKED FOR CORRECT CONTENTS.
.SBTL T0043
*****
T0043: SCOPE
```

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1989 010166 012706 001000      MOV      #1000,SP      ;SETUP THE STACK POINTER
1990 010172 004737 011730      JSR      PC,TORDER   ;MAKE SURE TESTS ARE IN PRPOER SEQUENCE
1991 010176 000043                00043                ;HERE LIES THE NUMBER OF THIS TEST
1992 010200 004737 013014      JSR      PC,LBOAT1   ;SET UP WRITE DATA (256 WORDS).
1993 010204 005077 171030      CLR      @TCCM
1994 010210 012777 020003 171022      MOV      @MAINT!UO!FWD!RNUM!DO,@TCCM
1995 010216                MTC00      MTK7,5
1996 010216 004537 012636      JSR      RS,LMTCC0   ;CALL LOAD MT CODES SUB.
1997 010222 033164                MTK7      ;ADDRESS OF MARK TRACK CODES.
1998 010224 000005                5              ;MARK TRACK CODE COUNT.
1999 010226 005777 171006      TST      @TCCM      ;ERROR BIT SET?
2000 010232 100002                BPL      R0043      ;BR IF NO ERROR.
2001 010234 104041                ERROR 41       ;ERROR BIT SET. EXAMINE TCST.
2002 010236 000457                BR         G0043
2003 010240 012777 177400 170774      MOV      #-256,@TCWC ; -256 TO WORD COUNT.
2004 010246 012777 036306 170770      MOV      @RBUF,@TCBA ; ADDR OF RBUF TO TCBA.
2005 010254 012704 037306                MOV      @RBUF+512,R4 ; ADDR TO SAVE TCDT DATA TO R4.
2006 010260 112777 000015 170752      MOV8     @DATA!DO,@TCCM ; ISSUE WDATA COMMAND.
2007 010266                MTC0E      H0043,MTK7A,262.
2008 010266 004537 013006      JSR      RS,LMTCC0E ; CALL LOAD MT CODES SUBROUTINE.
2009 010272 010404                H0043         ; ADDR TO GO AFTER EACH CODE PASSED.
2010 010274 033222                MTK7A        ; ADDRESS OF MARK TRACK CODES.
2011 010276 000406                262.         ; MARK TRACK CODE COUNT.
2012 010300 005777 170734      TST      @TCCM      ;ERROR BIT SET?
2013 010304 100002                BPL      B0043      ;BR IF NO ERROR.
2014 010306 104041                ERROR 41       ;ERROR BIT SET. EXAMINE TCST.
2015 010310 000432                BR         G0043
2016 010312 105777 170722      B0043:  TSTB     @TCCM      ;READY BIT SET?
2017 010316 100402                BMI      C0043      ;BR IF READY IS SET.
2018 010320 104067                ERROR 67       ;READY BIT FAILED TO SET.
2019 010322 000425                BR         G0043
2020 010324 005777 170712      C0043:  TST      @TCWC      ;WORD COUNT 0?
2021 010330 001407                BEQ      D0043      ;BR IF WORD COUNT IS 0.
2022 010332 017737 170704 001172      MOV      @TCWC,@REG4 ;PREPERE ERONIOUS WORD COUNT FOR PRINTOUT
2023 010340 005077 170616                CLR      @SREG0     ;PREPARE GOOD WORD COUNT INFO FOR PRINTOUT
2024 010344 104044                ERROR 44       ;WORD COUNT NOT 0.
2025 010346 000413                BR         G0043
2026 010350 022777 037306 170666      D0043:  CMP      @RBUF+512.,@TCBA ;TCBA CORRECT?
2027 010356 001402                BEQ      F0043      ;BR IF TCBA CORRECT.
2028 010360 104045                ERROR 45       ;TCBA INCORRECT. SHOULD BE RBUF+512.
2029 010362 000405                BR         G0043
2030 010364 004537 013130      F0043:  JSR      RS,CKDAT   ;COMPARE WRITE DATA AGAINST TCDT SAVED
2031 010370 001276                SBOAT1       ;DATA. REPORT ERRORS.
2032 010372 037306                RBUF+512.
2033 010374 000400                256.
2034 010376                G0043:
2035 010376 012706 001000      MOV      #1000,SP   ;RESTORE THE STACK POINTER
2036 010402 000403                BR         T0044    ;GO ON TO THE NEXT TEST
2037 010404 017724 170636      H0043:  MOV      @TCDT,(4)+ ;HERE AFTER EACH MARK CODE IS PASSED.
2038 010410 000002                RTI          ;SAVE TCDT DATA AND EXIT IOT TRAP.
2039                ;WRITE DATA COMPLEMENT OBVERSE TEST.
2040                .SBTTL T0044
2041                ;*****
2042 010412 000004      T0044:  SCOPE
2043 010414 012706 001000      MOV      #1000,SP   ;SETUP THE STACK POINTER
2044 010420 004737 011730      JSR      PC,TORDER   ;MAKE SURE TESTS ARE IN PRPOER SEQUENCE

```

H04

MAINDEC-11-DZTCB-D  
DZTCB0.P11 18-FEB-77

TC11 TEST #2  
10:59

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T0044

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2045 010424 000044          ; HERE LIES THE NUMBER OF THIS TEST
2046 010426 004737 013014  R0044: JSR    PC,LBOAT1 ; SET UP WRITE DATA (256 WORDS).
2047 010432 005077 170602          CLR    @TCCM
2048 010436 012777 024003 170574  MOV    #MAINT!UO!REV!RNUM!DO,@TCCM
2049 010444          MTCOD  MTK7,5
2050 010444 004537 012636          JSR    RS,LATCOD ; CALL LOAD MT CODES SUB.
2051 010450 033164          MTK7  ; ADDRESS OF MARK TRACK CODES.
2052 010452 000005          5 ; MARK TRACK CODE COUNT.
2053 010454 005777 170560          TST    @TCCM ; ERROR BIT SET?
2054 010460 100002          BPL   A0044 ; BR IF NO ERROR.
2055 010462 104041          ERROR 41 ; ERROR BIT SET EXAMINE TCST.
2056 010464 000432          BR    C0044
2057 010466 012777 177400 170546  A0044: MOV    #-256,@TCCW ; -256 TO WORD COUNT.
2058 010474 012777 036306 170542  MOV    #RBUF,@TCBA ; ADDR OF RBUF TO TCBA.
2059 010502 012704 037306          MOV    #RBUF+512,R4 ; ADDR TO SAVE TCDT DATA TO R4.
2060 010506 112777 000015 170524  MOVB  #WDATA!DO,@TCCM ; ISSUE WDATA COMMAND.
2061 010514          MTCOE  D0044,MTK7A,262.
2062 010514 004537 013006          JSR    RS,LMTCOE ; CALL LOAD MT CODES SUBROUTINE.
2063 010520 010560          D0044 ; ADDR TO GO AFTER EACH CODE PASSED.
2064 010522 033222          MTK7A ; ADDRESS OF MARK TRACK CODES.
2065 010524 000406          262. ; MARK TRACK CODE COUNT.
2066 010526 005777 170506          TST    @TCCM ; ERROR BIT SET?
2067 010532 100002          BPL   B0044 ; BR IF NO ERROR.
2068 010534 104041          ERROR 41 ; ERROR BIT SET. EXAMINE TCST.
2069 010536 000405          BR    C0044
2070 010540 004537 013130  B0044: JSR    RS,CKDAT ; CHECK THAT SAVED TCDT DATA WAS COMPLEMENT
2071 010544 001306          SBOAT3 ; OBSERVED CORRECTLY.
2072 010546 037306          RBUF+512.
2073 010550 000400          256.
2074 010552          C0044:
2075 010552 012706 001000          MOV    #1000,SP ; RESTORE THE STACK POINTER
2076 010556 000403          BR    T0045 ; GO ON TO THE NEXT TEST
2077 010560 017724 170462  D0044: MOV    @TCDT,(4)+ ; HERE AFTER EACH MARK CODE IS PASSED.
2078 010564 000002          RTI ; SAVE TCDT DATA AND EXIT IOT TRAP.
2079
2080 ; WRITE ALL TEST.
2081 .SBTTL T0045
2082 *****
2083 010566 000004          T0045: SCOPE
2084 010570 012706 001000          MOV    #1000,SP ; SETUP THE STACK POINTER
2085 010574 004737 011730          JSR    PC,TORDER ; MAKE SURE TESTS ARE IN PROPER SEQUENCE
2086 010600 000045          D0045 ; HERE LIES THE NUMBER OF THIS TEST
2087 010602 004737 013014  R0045: JSR    PC,LBOAT1 ; SET UP WRITE DATA.
2088 010606 005077 170426          CLR    @TCCM
2089 010612 012777 020003 170420  MOV    #MAINT!UO!FWD!RNUM!DO,@TCCM
2090 010620          MTCOD  MTK7,4
2091 010620 004537 012636          JSR    RS,LATCOD ; CALL LOAD MT CODES SUB.
2092 010624 033164          MTK7  ; ADDRESS OF MARK TRACK CODES.
2093 010626 000004          4 ; MARK TRACK CODE COUNT.
2094 010630 005777 170404          TST    @TCCM ; ERROR BIT SET?
2095 010634 100002          BPL   A0045 ; BR IF NO ERROR.
2096 010636 104041          ERROR 41 ; ERROR BIT SET. EXAMINE TCST.
2097 010640 000470          BR    G0045
2098 010642 005077 170374  A0045: CLR    @TCCW ; 0 TO WORD COUNT.
2099 010646 012777 036306 170370  MOV    #RBUF,@TCBA ; ADDR OF RBUF TO TCBA.
2100 010654 012703 036304          MOV    #RBUF-2,R3
2100 010660 012704 037306          MOV    #RBUF+512.,R4

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2101 010664 012737 000402 001274      MOV      #258, CTRA      ; # OF WORDS TO WRITE TO CTRA.
2102 010672 004737 012136      JSR      PC, STICV      ; SET INTERRUPT VECTOR TO IIC.
2103 010676 010720      B0045
2104 010700 112777 000117 170332      MOVB     #WALL!IE!DO, @TCCM; ISSUE WRITE ALL COMMAND. INTERRUPT ENABLED.
2105 010706 004537 013006      MTCOE    I0045, MTK5, 260.
2106 010706 004537 013006      JSR      RS, LMTCOE      ; CALL LOAD MT CODES SUBROUTINE.
2107 010712 011030      I0045      ; ADDR TO GO AFTER EACH CODE PASSED.
2108 010714 033214      MTK5      ; ADDRESS OF MARK TRACK CODES.
2109 010716 000404      260.      ; MARK TRACK CODE COUNT.
2110 010720 005777 170314      B0045:   TST      @TCCM      ; ERROR BIT SET?
2111 010724 100002      BPL      B0045A      ; BR IF NO ERROR.
2112 010726 104041      ERROR 41      ; ERROR BIT SET. EXAMINE TCST.
2113 010730 000434      BR
2114 010732 012377 170310      B0045A:  MOV      (3)+, @TCDT      ; WRITE DATA TO TCDT.
2115 010736 005337 001274      DEC      CTRA      ; WROTE 257 WORDS?
2116 010742 001401      BEQ      C0045      ; BR IF 257 WORDS WRITTEN.
2117 010744 000002      RTI
2118 010745 005737 037306      C0045:   TST      @RBUF+512.      ; NOT DONE. EXIT INTERRUPT.
2119 010752 001404      BEQ      D0045      ; 1ST WORD WRITTEN EQUAL 0?
2120 010754 005037 001162      CLR      $REGO      ; BR IF FIRST WORD 0.
2121 010760 104070      ERROR 70      ; 1ST WORD WRITTEN NOT 0. (REV CHECKSUM).
2122 010762 000417      BR
2123 010764 004537 013130      D0045:   JSR      RS, CKDAT      ; CHECK THAT SAVED TCDT DATA MATCHES
2124 010770 001276      SBDAT1      ; WRITE DATA.
2125 010772 037310      RBUF+514.
2126 010774 000400      256.
2127 010776 005777 170240      TST      @TCCM      ; WORD COUNT STILL 0?
2128 011002 001402      BEQ      F0045      ; BR IF WORD COUNT IS 0.
2129 011004 104071      ERROR 71      ; WORD COUNT MODIFIED DURING WRITE ALL.
2130 011006 000405      BR
2131 011010 022777 036306 170226      F0045:   CMP      @RBUF, @TCBA      ; TCBA STILL EQUAL RBUF?
2132 011016 001401      BEQ      G0045      ; BR IF TCBA STILL SAME.
2133 011020 104072      ERROR 72      ; TCBA MODIFIED DURING WRITE ALL.
2134 011022      G0045:
2135 011022 012706 001000      MOV      #1000, SP      ; RESTORE THE STACK POINTER
2136 011026 000403      BR      T0046      ; GO ON TO THE NEXT TEST
2137 011030 017724 170212      I0045:   MOV      @TCDT, (4)+      ; HERE AFTER EACH MARK CODE IS PASSED.
2138 011034 000002      RTI      ; SAVE TCDT DATA AND EXIT IOT TRAP.
2139
2140      .SBTTL T0046
2141      ;*****
2142 011036 000004      T0046:   SCOPE
2143 011040 012706 001000      MOV      #1000, SP      ; SETUP THE STACK POINTER
2144 011044 004737 011730      JSR      PC, TORDER      ; MAKE SURE TESTS ARE IN PRPOER SEQUENCE
2145 011050 000046      00046      ; HERE LIES THE NUMBER OF THIS TEST
2146 011052 004537 013256      R0046:   JSR      RS, CKSELE      ; SST TO U1.
2147 011056 000400      U1
2148 011060 104073      ERROR 73      ; SST TO U1 DID NOT CAUSE SELECT ERROR.
2149
2150 011062 012706 001000      MOV      #1000, SP      ; RESTORE THE STACK POINTER
2151 011066 000400      BR      T0047      ; GO ON TO THE NEXT TEST
2152      .SBTTL T0047
2153      ;*****
2154 011070 000004      T0047:   SCOPE
2155 011072 012706 001000      MOV      #1000, SP      ; SETUP THE STACK POINTER
2156 011076 004737 011730      JSR      PC, TORDER      ; MAKE SURE TESTS ARE IN PRPOER SEQUENCE

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2157 011102 000047
2158 011104 004537 013256
2159 011110 001000
2160 011112 104073
2161
2162 011114 012706 001000
2163
2164
2165 011120 000004
2166 011122 012706 001000
2167 011126 004737 011730
2168 011132 000050
2169 011134 004537 013256
2170 011140 001400
2171 011142 104073
2172
2173 011144 012706 001000
2174
2175
2176 011150 000004
2177 011152 012706 001000
2178 011156 004737 011730
2179 011162 000051
2180 011164 004537 013256
2181 011170 002000
2182 011172 104073
2183
2184 011174 012706 001000
2185
2186
2187 011200 000004
2188 011202 012706 001000
2189 011206 004737 011730
2190 011212 000052
2191 011214 004537 013256
2192 011220 002400
2193 011222 104073
2194
2195 011224 012706 001000
2196
2197
2198 011230 000004
2199 011232 012706 001000
2200 011236 004737 011730
2201 011242 000053
2202 011244 004537 013256
2203 011250 003000
2204 011252 104073
2205 011254 000240
2206 011256 000240
2207 011260 000240
2208
2209 011262 012706 001000
2210
2211
2212 011266 000004

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00047
R0047: JSR R5,CKSELE ;HERE LIES THE NUMBER OF THIS TEST
U2 ;SST TO U2.
ERROR 73 ;SST TO U2 DID NOT CAUSE SELECT ERROR.

MOV #1000,SP ;RESTORE THE STACK POINTER
.SBTTL T0050
*****
T0050: SCOPE
MOV #1000,SP ;SETUP THE STACK POINTER
JSR PC,TORDER ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
00050 ;HERE LIES THE NUMBER OF THIS TEST
R0050: JSR R5,CKSELE ;SST TO U1.
U3 ;SST TO U3 DID NOT CAUSE SELECT ERROR.
ERROR 73

MOV #1000,SP ;RESTORE THE STACK POINTER
.SBTTL T0051
*****
T0051: SCOPE
MOV #1000,SP ;SETUP THE STACK POINTER
JSR PC,TORDER ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
00051 ;HERE LIES THE NUMBER OF THIS TEST
R0051: JSR R5,CKSELE ;ISSUE A SST COMMAND
U4 ;SST TO U4 DID NOT CAUSE SELECT ERROR.
ERROR 73

MOV #1000,SP ;RESTORE THE STACK POINTER
.SBTTL T0052
*****
T0052: SCOPE
MOV #1000,SP ;SETUP THE STACK POINTER
JSR PC,TORDER ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
00052 ;HERE LIES THE NUMBER OF THIS TEST
R0052: JSR R5,CKSELE ;ISSUE A SST COMMAND
U5 ;SST TO U5 DID NOT CAUSE SELECT ERROR.
ERROR 73

MOV #1000,SP ;RESTORE THE STACK POINTER
.SBTTL T0053
*****
T0053: SCOPE
MOV #1000,SP ;SETUP THE STACK POINTER
JSR PC,TORDER ;MAKE SURE TESTS ARE IN PROPER SEQUENCE
00053 ;HERE LIES THE NUMBER OF THIS TEST
R0053: JSR R5,CKSELE ;ISSUE A SST COMMAND
U6 ;SST TO U6 DID NOT CAUSE SELECT ERROR.
ERROR 73
NOP
NOP
NOP

MOV #1000,SP ;RESTORE THE STACK POINTER
.SBTTL T0054
*****
T0054: SCOPE

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K04

MAINDEC-11-DZTCB-D TC11 TEST #2  
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T0054

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2213 011270 012706 001000      MOV      #1000,SP      ; SETUP THE STACK POINTER
2214 011274 004737 011730      JSR      PC,TORDER    ; MAKE SURE TESTS ARE IN PROPER SEQUENCE
2215 011300 000054              00054              ; HERE LIES THE NUMBER OF THIS TEST
2216 011302 004537 013256      RO054: JSR      RS,CKSELE ; ISSUE A SST COMMAND
2217 011306 003400              U7
2218 011310 104073              ERROR 73           ; SST TO U7 DID NOT CAUSE SELECT ERROR.
2219
2220 011312 012706 001000      MOV      #1000,SP      ; RESTORE THE STACK POINTER
2221 .SHTTL T0055
2222 *****
2223 011316 000004      T0055: SCOPE
2224 011320 012706 001000      MOV      #1000,SP      ; SETUP THE STACK POINTER
2225 011324 004737 011730      JSR      PC,TORDER    ; MAKE SURE TESTS ARE IN PROPER SEQUENCE
2226 011330 000055              00055              ; HERE LIES THE NUMBER OF THIS TEST
2227 011332 004737 013046      JSR      PC,LBBIND    ; LOAD BUFFER WITH BINARY DATA.
2228 011336 005077 167676      CLR      @TCCH
2229 011342 012777 020003 167670      MOV      #MAINT!UD!FWD!RNUM!DO,@TCCH
2230 011350              MTCOD
2231 011350 004537 012636      JSR      RS,LATCOD    ; CALL LOAD MT CODES SUB.
2232 011354 033164              MTK7              ; ADDRESS OF MARK TRACK CODES.
2233 011356 000005              5                ; MARK TRACK CODE COUNT.
2234 011360 005777 167654      TST      @TCCH       ; ERROR BIT SET?
2235 011364 100002      BPL      R0055       ; BR IF NO ERROR.
2236 011366 104041      ERROR 41           ; ERROR BIT SET. EXAMINE TCST.
2237 011370 000441      BR
2238 011372 012777 177400 167642      RO055: MOV      #-256,@TCWC   ; -256 TO WORD COUNT.
2239 011400 012777 036306 167636      MOV      #RBUF,@TCBA  ; RBUF ADDR TO TCBA.
2240 011406 012704 037306      MOV      #RBUF+512.,R4 ; ADDR TO SAVE TCDT DATA TO R4.
2241 011412 112777 000015 167620      MOV      #DATA!DO,@TCCH ; ISSUE WRITE DATA COMMAND.
2242 011420              MTCOE
2243 011420 004537 013006      JSR      RS,LATCOE   ; CALL LOAD MT CODES SUBROUTINE.
2244 011424 011502      FO055            ; ADDR TO GO AFTER EACH CODE PASSED.
2245 011426 033222      MTK7A           ; ADDRESS OF MARK TRACK CODES.
2246 011430 000406      262.           ; MARK TRACK CODE COUNT.
2247 011432 005777 167602      TST      @TCCH       ; ERROR BIT SET?
2248 011436 100002      BPL      BO055       ; BR IF NO ERROR.
2249 011440 104044      ERROR 44           ; ERROR BIT SET. EXAMINE TCST.
2250 011442 000414      BR
2251 011444 012701 037306      BO055: MOV      #RBUF+512.,R1 ; ADDR OF DATA TO CHECK TO R1.
2252 011450 012703 036306      MOV      #RBUF,R3     ; ADDR OF EXPECTED DATA TO R3.
2253 011454 012702 000400      MOV      #256.,R2    ; # OF WORDS TO CHECK TO R2.
2254 011460 005037 013254      CLR      WDCNT
2255 011464 004737 013202      CO055: JSR      PC,COTCK  ; CHECK DATA WORD.
2256 011470 005302      DEC      R2          ; ALL WORDS CHECKED?
2257 011472 001374      BNE      CO055       ; BR IF NOT DONE YET.
2258 011474
2259 011474 012706 001000      DO055: MOV      #1000,SP      ; RESTORE THE STACK POINTER
2260 011500 000403      BR      T0056
2261 011502 017724 167540      FO055: MOV      @TCDT,(4)+ ; GO ON TO THE NEXT TEST
2262 011506 000002      RTI              ; HERE AFTER EACH MARK CODE IS PASSED.
2263 ; SAVE TCDT DATA AND EXIT.
2264 .SHTTL T0056
2265 011510 000004      T0056: SCOPE
2266 011512      .SEOP STARTX,PASCNT
2267 .SHTTL END OF PASS ROUTINE
2268

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2269 011512 STARS
2270 ;*****
2271 ;INCREMENT THE PASS NUMBER ($PASS)
2272 ;*TYPE "END PASS #XXXXX" (WHERE XXXXX IS A DECIMAL NUMBER)
2273 ;*IF THERES A MONITOR GO TO IT
2274 ;*IF THERE ISN'T JUMP TO STARTX
2275
2276 011512 SEOP:
2277 011512 000004 .LIST SCOPE
2278
2279 011514 005037 001102 CLR $STNM ;ZERO THE TEST NUMBER
2280 011520 005037 001222 CLR $TIMES ;ZERO THE NUMBER OF ITERATIONS
2281 011524 005237 001100 INC $PASS ;INCREMENT THE PASS NUMBER
2282 011530 042737 100000 001100 BIC #100000,$PASS ;DON'T ALLOW A NEG. NUMBER
2283 011536 005327 DEC (PC)+ ;LOOP?
2284 011540 000001 SEOPCT: .WORD 1
2285 011542 003022 BGT $DOAGN ;YES
2286 011544 012737 MOV (PC)+,@(PC)+ ;RESTORE COUNTER
2287 011546 000001 SENDCT: .WORD 1
2288 011550 011540 SEOPCT
2289 011552 104401 011617 TYPE $ENDMG ;TYPE "END PASS #"
2290 011556 TYPDEC $PASS
2291 011556 013746 001100 MOV $PASS,-(SP) ;SAVE $PASS FOR TYPEOUT
2292 011562 104405 TYPDS ;GO TYPE--DECIMAL ASCII WITH SIGN
2293 011564 104401 011614 TYPE $NULL ;TYPE A NULL CHARACTER
2294 011570 013700 000042 $GET42: MOV @#42,RO ;GET MONITOR ADDRESS
2295 011574 001405 BEQ $DOAGN ;BRANCH IF NO MONITOR
2296
2297 011576 000005 .LIST RESET ;CLEAR THE WORLD
2298 011600 004710 SENDAD: JSR PC,(RO) ;GO TO MONITOR
2299 011602 000240 NOP ;SAVE ROOM
2300 011604 000240 NOP ;FOR
2301 011606 000240 NOP ;ACT11
2302
2303 011610 000137 $DOAGN: JMP @(PC)+ ;RETURN
2304 011612 002574 $RTNAD: .WORD STARTX
2305 011614 377 377 000 $NULL: .BYTE -1,-1,0 ;NULL CHARACTER STRING
2306 011617 015 042412 042116 $ENDMG: .ASCIZ <15><12>/END PASS #/
2307 011624 050040 051501 020123
2308 011632 000043
2309
2310 011634 012737 015717 011672 ;* THIS ROUTINE HANDLES FATAL TRAP ERRORS
2311 011642 000403 TRAP10: MOV #TRPM10,TMESAD ;ADDRESS OF TRAP TO 10 MESSAGE TO THE MESSAGE PO
2312 011644 012737 015575 011672 BR TRAPX ;ENTER THE FATAL TRAP ERRGR REPORT ROUTINE
2313 011652 011600 TRAP4: MOV #TRPM45,TMESAD
2314 011654 162700 000002 TRAPX: MOV (SP),RO ;SAVE PC OF WHERE TRAP OCCURRED
2315 011660 012706 001000 SUB #2,RO ;MAKE IT POINT EXACTLY AT THE OFFENDING WORD
2316 011664 005046 MOV #1000,SP ;MAKE SURE THAT THE STACK GIVES NO PROBLEMS
2317 011666 004737 014230 CLR -(SP) ;FAKEOUT THE PRINTOUT ROUTINE
2318 011672 000000 TMESAD: JSR PC,$TYPE ;PRINT THE TRAP MESSAGE
2319 011674 010016 MOV RO,(SP) ;ADDRESS OF THE TRAP MESSAGE GOES HERE
2320 011676 104402 TYPDC ;PUT ERROR PC BACK ONTO THE STACK
2321 011700 104401 001233 TRYAGN: TYPE $CRLF
2322 011704 104401 015645 TYPE ,TRPMES ;THEN PRINTOUT THE TRAP MESSAGE
2323 011710 000240 NOP ;PATCHING SPACE, THOUGHTFULLY PROVIDED
2324 011712 000240 NOP ;PATCHING SPACE, THOUGHTFULLY PROVIDED

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2325 011714 000240      NOP      ;PATCHING SPACE, THOUGHTFULLY PROVIDED
2326 011716 000240      NOP      ;PATCHING SPACE, THOUGHTFULLY PROVIDED
2327 011720 000240      NOP      ;PATCHING SPACE, THOUGHTFULLY PROVIDED
2328 011722 000005      RESET
2329 011724 000137 002312  JMP      @#START
2330                                     ;SUBROUTINE TO CHECK TO MAKE SURE THAT EACH TEST IN
2331                                     ;RUNNING WHEN IT SHOULD
2332 011730 011637 001162  TORDER: MOV    #2,SP      ;GET ADDRESS OF TEST #
2333 011734 062716 000002      ADD    #2,SP      ;BUMP RETURN ADDRESS TO HOP OVER THE IN LINE TEST #
2334 011740 123777 001102 167214  CMPB   $TSTM,$SREG0 ;FIND OUT IF THE TEST #'S MATCH
2335 011746 001410      BEQ    TORDER      ;IF THEY DO HOP OVER THE ERROR SIGNAL STUFF
2336 011750 013737 001162 001164  MOV    $SREG0,$REG1 ;SAVE ADDRESS OF TEST
2337 011756 017737 167200 001162  MOV    $SREG0,$SREG0 ;GET TEST# WAS DATA READY FOR PRINTOUT
2338 011764 104026      ERROR   26         ;PRINTOUT "OUT OF ORDER" MESSAGE
2339 011766 000744      BR     TRYAGN      ;GO TRY TO START OVER
2340 011770 000207      TORDER: RTS    PC      ;RETURN
2341                                     ;SAVE REGS 0 TO 4 SUBROUTINE.
2342 011772 012666 177764  SV04:  MOV    (6)+,-12.(6) ;MOVE PC UPSTACK.
2343 011776 012737 000207 012050  MOV    #RTSPC,SV05C
2344 012004 000412      BR     SV05B
2345                                     ;SUB TO SAVE REGS 0 TO 5 AND PLACE JSR PC IN R5.
2346 012006 012737 000240 012050  SV05S: MOV    #NOP,SV05C
2347 012014 000403      BR     SV05A
2348                                     ;SUB TO SAVE REGS 0 TO 5.
2349 012016 012737 000207 012050  SV05:  MOV    #RTSPC,SV05C
2350 012024 012666 177762  SV05A: MOV    (6)+,-14.(6) ;MOVE PC UPSTACK.
2351 012030 010546      MOV    R5,-(6)
2352 012032 010446      SV05B: MOV    R4,-(6)
2353 012034 010346      MOV    R3,-(6)
2354 012036 010246      MOV    R2,-(6)
2355 012040 010146      MOV    R1,-(6)
2356 012042 010046      MOV    R0,-(6)
2357 012044 162706 000002  SUB    #2,SP
2358 012050 000207  SV05C: RTS    PC      ;RTS PC OR NOP.
2359 012052 016605 000016      MOV    14.(6),R5 ;JSR PC TO R5.
2360 012056 000207      RTS    PC      ;EXIT.
2361                                     ;RESTORE REGS 0 TO 4 SUBROUTINE.
2362 012060 062706 000002  RS04:  ADD    #2,SP
2363 012064 012600      MOV    (6)+,R0 ;RESTORE REGS 0 TO 4.
2364 012066 012601      MOV    (6)+,R1
2365 012070 012602      MOV    (6)+,R2
2366 012072 012603      MOV    (6)+,R3
2367 012074 012604      MOV    (6)+,R4
2368 012076 016646 177764  MOV    -12.(6),-(6) ;MOVE PC DOWN STACK.
2369 012102 000207      RTS    PC      ;EXIT
2370                                     ;SUB TO SET R5 IN EMT PC AND RESTORE REGS 0 TO 5.
2371 012104 010566 000016  RS05S: MOV    R5,14.(6) ;SET EMT PC TO R5 CONTENTS.
2372                                     ;SUB TO RESTORE REGS 0 TO 5.
2373 012110 062706 000002  RS05:  ADD    #2,SP
2374 012114 012600      MOV    (6)+,R0
2375 012116 012601      MOV    (6)+,R1
2376 012120 012602      MOV    (6)+,R2
2377 012122 012603      MOV    (6)+,R3
2378 012124 012604      MOV    (6)+,R4
2379 012126 012605      MOV    (6)+,R5
2380 012130 016646 177762  MOV    -14.(6),-(6) ;MOVE PC DOWNSTACK.
    
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2381	012134	000207		RTS	PC	;EXIT
2382	012136	004737	012006	:ROUTINE TO SET	TC11 INTERRUPT VECTOR AND PRIORITY	
2383	012142	013701	001250	STTCV: JSR	PC, SVOSS	
2384	012146	012521		MOV	TCVTR, R1	;VECTOR TO R1.
2385	012150	013721	001252	MOV	(5)+, (1)+	;SET DESIRED VECTOR.
2386	012154	004737	012104	MOV	TCLVL, (1)+	;SET TC11 PRIORITY.
2387	012160	000207		JSR	PC, RS055	
2388				RTS	PC	
2389				:ROUTINE TO ISSUE RESET.		
2390	012162	010046		SRSETT: MOV	RO, -(6)	;PUSH RO.
2391	012164	012700	052525	MOV	#52525, RO	;DATA TO RO.
2392	012170	005100		COM	RO	;COMPLEMENT (RO).
2393	012172	010037	012166	MOV	RO, SRSETT+4	; (RO) TO SRSETT+4.
2394	012176	000005		RESET		;ISSUE RESET. (RO) IS
2395	012200	012600		MOV	(6)+, RO	;RESTORE RO.
2396	012202	000207		RTS	PC	;EXIT
2397	012204	004537	012610	RSTMTK: JSR	RS, BMOVE	;RESTORE MTKVAR MARK CODE.
2398	012210	033126		MTKC10		;AND GOOD CHECKSUM.
2399	012212	033236		MTKVAR		
2400	012214	000006		6		
2401	012216	004537	012610	JSR	RS, BMOVE	
2402	012222	033156		MTKSP		
2403	012224	033214		MTKS		
2404	012226	000006		6		
2405	012230	004537	012610	JSR	RS, BMOVE	
2406	012234	036267		GCKSM		
2407	012236	036230		FCKSM		
2408	012240	000006		6		
2409	012242	000207		RTS	PC	;EXIT.
2410				:COMMON HALT ROUTINE		
2411	012244	004737	012006	CHLT: JSR	PC, SVOSS	
2412	012250	010500		MOV	RS, RO	;DEVELOP ADDR OF CALLER.
2413	012252	005740		TST	-(0)	
2414	012254	000000		HALT		;HALT CALL ADDR IN DATA LIGTHS.
2415	012256	004737	012104	JSR	PC, RS055	
2416	012262	000207		RTS	PC	;EXIT.
2417				:RANDOM NUMBER GENERATOR. ROUTINE EXITS WITH NUMBER IN REGISTER 0.		
2418	012264	013700	012332	RNGEN: MOV	RP1, RO	
2419	012270	006100		ROL	RO	
2420	012272	006100		ROL	RO	
2421	012274	063700	012334	ADD	RP2, RO	
2422	012300	010037	012332	MOV	RO, RP1	
2423	012304	006100		ROL	RO	
2424	012306	006100		ROL	RO	
2425	012310	063700	012334	ADD	RP2, RO	
2426	012314	006100		ROL	RO	
2427	012316	006100		ROL	RO	
2428	012320	010037	012334	MOV	RO, RP2	
2429	012324	013700	012332	MOV	RP1, RO	
2430	012330	000207		RTS	PC	;EXIT. NUMBER IN RO
2431	012332	001233		RP1:	1233	
2432	012334	007622		RP2:	7622	
2433				:SUBROUTINE TO DELAY A SPECIFIED NUMBER OF MILLISECONDOS		
2434	012336	004737	012006	DLY: JSR	PC, SVOSS	
2435	012342	012500		MOV	(5)+, RO	;DELAY COUNT TO RO.
2436	012344	005037	177776	CLR	PSW	;SET PRIORITY 0.

2437	012350	012701	000226		DLYA: MOV #226,R1 ; 1 MSEC COUNT TO R1.
2438	012354	005301			DLYB: DEC R1 ; DECREMENT 1 MSEC COUNT.
2439	012356	001376			BNE DLYB ; BR IF NOT 0.
2440	012360	005300			DEC RO ; DECREMENT DELAY COUNT.
2441	012362	001372			BNE DLYA ; BR IF NOT DONE DELAYING.
2442	012364	004737	012104		JSR PC,RSOSS
2443	012370	000207			RTS PC ; EXIT.
2444					; SUBROUTINE TO STALL A RANDOM NUMBER OF MILLISECONDS. MAXIMUM STALL
2445					; DETERMINED BY CONTENTS OF LOC STLMSK.
2446	012372	004737	012006		STAL: JSR PC,SVOSS ; GO GET RANDOM NUMBER.
2447	012376	004737	012264		JSR PC,RNGEN ; 8 IN RO. APPLY STALL MASK.
2448	012402	043700	012430		BIC STLMSK,RO ; BRANCH IF RESULT IS 0.
2449	012406	001407			BEB STALB
2450	012410	010037	012420		MOV RO,STALA ; DELAY
2451	012414	004737	012336		JSR PC,DLY ; DELAY COUNT
2452	012420	000000			STALA: OPEN ; DELAY COUNT
2453	012422	004737	012104		JSR PC,RSOSS
2454	012426	000207			STALB: RTS PC ; DONE. EXIT.
2455	012430	000000			STLMSK: OPEN ; STALL MASK.
2456					; SUBROUTINE TO CLEAR DECTAPE READ BUFFER.
2457	012432	005037	036306		CLRBUF: CLR RBUF ; CLEAR 512 WORD READ BUFFER.
2458	012436	004537	012610		JSR RS,BMOVE ; TO ALL 0'S.
2459	012442	036306			RBUF
2460	012444	036307			RBUF+1
2461	012446	001777			1023.
2462	012450	000207			RTS PC ; EXIT.
2463					; SUBROUTINE TO INITIALIZE BINARY COUNT PATTERNS
2464	012452	012737	177777	012474	INBIN: MOV #-1,RIND ; SET ALL VARIABLES
2465	012460	004537	012610		JSR RS,BMOVE ; TO MINUS 1.
2466	012464	012474			RIND
2467	012466	012475			RIND+1
2468	012470	000013			11.
2469	012472	000207			RTS PC ; EXIT
2470	012474	000000			RIND: OPEN
2471	012476	000000			PTO: OPEN
2472	012500	000000			PT1: OPEN
2473	012502	000000			PIND: OPEN
2474	012504	000000			PTOP: OPEN
2475	012506	000000			PTIP: OPEN
2476					; SPECIAL BINARY COUNT PATTERN SUBROUTINE. EXITS WITH BIN CHAR IN RO
2477	012510	013737	012476	012500	GTBIN: MOV PTO,PT1 ; PREVIOUS BIN CHAR TO PT1
2478	012516	005137	012500		COM PT1
2479	012522	005137	012474		COM RIND
2480	012526	001002			BNE .+6
2481	012530	005237	012500		INC PT1
2482	012534	013737	012500	012476	MOV PT1,PTO ; SAVE BIN CHAR IN PTO
2483	012542	013700	012500		MOV PT1,RO ; BIN CHAR TO RO.
2484	012546	000207			RTS PC ; EXIT.
2485	012550	013737	012504	012506	GTBINP: MOV PTO,PTIP ; PREVIOUS BIN CHAR TO PTIP
2486	012556	005137	012506		COM PTIP
2487	012562	005137	012502		COM PIND
2488	012566	001002			BNE .+6
2489	012570	005237	012506		INC PTIP
2490	012574	013737	012506	012504	MOV PTIP,PTOP ; SAVE BIN CHAR IN PTO.
2491	012602	013701	012506		MOV PTIP,R1 ; BIN CHAR TO R1.
2492	012606	000207			RTS PC ; EXIT.

25493	012610	004737	011772						
25494	012614	012501							
25495	012616	012502							
25496	012620	012503							
25497	012622	112122							
25498	012624	005303							
25499	012626	001375							
25500	012630	004737	012060						
25501	012634	000205							
25502									
25503									
25504	012636	005037	001260						
25505	012642	012537	012776						
25506	012646	012537	013002						
25507	012652	052777	020000	166360					
25508	012660	013737	013002	013004					
25509	012666	013701	001236						
25510	012672	012702	000100						
25511	012676	013700	012776						
25512	012702	012737	000006	013000					
25513	012710	111011							
25514	012712	150210							
25515	012714	111011							
25516	012716	111011							
25517	012720	140210							
25518	012722	112011							
25519	012724	005337	013000						
25520	012730	001413							
25521	012732	022737	000002	013000					
25522	012740	001363							
25523	012742	005737	001260						
25524	012746	001760							
25525	012750	005046							
25526	012752	004777	166302						
25527	012756	000754							
25528	012760	005337	013004						
25529	012764	001001							
25530	012766	000205							
25531	012770	105710							
25532	012772	100343							
25533	012774	000740							
25534	012776	000000							
25535	013000	000000							
25536	013 12	000000							
25537	013 14	000000							
25538	013006	012537	001260						
25539	013012	000713							
25540	013014	004737	012432						
25541	013020	004537	012610						
25542	013024	001276							
25543	013026	036306							
25544	013030	000004							
25545	013032	004537	012610						
25546	013036	036306							
25547	013040	036312							
25548	013042	000774							

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; SUBROUTINE TO MOVE A VARIABLE NUMBER OF BYTES.
BMOVE: JSR PC, SVD4 ; SAVE REGS.
        MOV (5)+, R1 ; GET FROM ADDRESS
        MOV (5)+, R2 ; GET TO ADDRESS
        MOV (5)+, R3 ; GET COUNT
BMOVA: MOVB (1)+, (2)+ ; MOVE BYTE
        DEC R3 ; DECREMENT COUNT
        BNE BMOVA ; BRANCH IF NOT DONE.
        JSR PC, RSD4 ; RESTORE REGS.
        RTS ; DONE EXIT

; SUB TO PASS TIMING, MARK, AND DATA TO TC11 CONTROL UNDER MAINTENANCE MODE.
LMTCD: CLR COCAL ; DO NOT CALL CODE AFTER EACH MARK
LMTCAA: MOV (5)+, MTKADR ; GET MARK TRACK ADDRESS.
        MOV (5)+, CDCNT ; GET NTH CODE COUNT.
        BIS #BIT13, BTCCM ; SET MAINTENANCE BIT.
        MOV CDCNT, CDCTR ; CODE COUNT TO CODE COUNTER.
        MOV TCST, R1 ; ADDR CONTAINING TCST ADDR TO R1.
        MOV #100, R2
LMTCA: MOV MTKADR, R0 ; MARK TRACK ADDR TO R0.
LMTCB: MOV #6, BTCTR ; 6 TO BIT COUNTER.
LMTCC: MOVB (0), (1) ; SET MARK TRACK BIT AND DATA.
        BISB R2, (0)
        MOVB (0), (1) ; TPI. LOADS MARK TRACK.
        BICB R2, (0) ; RELOAD DATA.
        MOVB (0)+, (1) ; TPO. SHIFTS DATA IN RMB.
        DEC BTCTR ; 6TH BIT SET?
        BEQ LMTCE ; BR IF 6TH BIT SET.
        CMP #2, BTCTR ; NOT 6TH. 4TH BIT SET?
        BNE LMTCC ; BRANCH IF NOT.
        TST COCAL ; DO WE WANT TO CALL CODE
        BEQ LMTCC ; DO NOT IF CODE CALL SWITCH = 0
        CLR -(6) ; IF ITS NOT =0 FAKE A INTERRUPT
        JSR PC, @COCAL ; TO LOCATION SPECIFIED IN CODE CALL SWITCH
        BR LMTCC
LMTCE: DEC CDCTR ; NTH CODE SET?
        BNE LMTCD ; BRANCH IF NOT.
        RTS ; EXIT.
LMTCD: TSTB @R0 ; LAST CODE?
        BPL LMTCB ; BRANCH IF NOT LAST CODE.
        BR LMTCA ; LAST CODE.

MTKADR: OPEN
BTCTR: OPEN
CDCNT: OPEN
CDCTR: OPEN
LMTCOE: MOV (5)+, COCAL ; SAVE ADDRESS TO GO TO AFTER EACH MARK
        BR LMTCAA
LBDAT1: JSR PC, CLRBUF ; CLEAR BUFFER AREA.
        JSR R5, BMOVE ; LOAD 256 WORD BUFFER WITH SBDAT1 DATA.
        SBDAT1
        RBUF
        4
        JSR R5, BMOVE
        RBUF
        RBUF+4
        SOB.
    
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2605 013324 .SSCOPE 4,SCOMAC
2606 .SBTTL SCOPE HANDLER ROUTINE
2607
2608 013324 STARS
2609 *****
2610 ;THIS ROUTINE CONTROLS THE LOOPING OF SUBTESTS. IT WILL INCREMENT
2611 ;AND LOAD THE TEST NUMBER($STNM) INTO THE DISPLAY REG.(DISPLAY<7:0>)
2612 ;AND LOAD THE ERROR FLAG ($ERFLG) INTO DISPLAY<15:08>
2613 ;THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:
2614 ;SW14=1 LOOP ON TEST
2615 ;SW11=1 INHIBIT ITERATIONS
2616 ;SW09=1 LOOP ON ERROR
2617 .LIST
2618 ;SW08=1 LOOP ON TEST IN SWR<7:0>
2619 ;CALL
2620 ;* SCOPE ;;SCOPE=IOT
2621
2622 013324 $SCOPE:
2623 .IRP NEWINS,<SCOMAC>
2624 NEWINS
2625 .ENDM
2626 SCOMAC
2627 013324 005077 165710 CLR @TCCM
2628 013330 005066 000002 CLR 2(SP) ;PS TO =0 AFTER WE EXIT THE SCOPE ROUTINE
2629 013334 004737 012162 JSR PC,$RSETT
2630 013340 004737 012204 JSR PC,$RSTMTK
2631 013344 032777 040000 15: BIT @BIT14,@SWR ;;LOOP ON PRESENT TEST?
2632 013352 001111 BNE $OVER ;;YES IF SW14=1
2633 ;*****START OF CODE FOR THE XOR TESTER*****
2634 013354 000416 $XTSTR: BR 6$ ;;IF RUNNING ON THE "XOR" TESTER CHANGE
2635 ;THIS INSTRUCTION TO A "NOP" (NOP=240)
2636 013356 013746 000004 MOV @ERRVEC,-(SP) ;;SAVE THE CONTENTS OF THE ERROR VECTOR
2637 013362 012737 013402 000004 MOV @SS,@ERRVEC ;;SET FOR TIMEOUT
2638 013370 005737 177060 TST @177060 ;;TIME OUT ON XOR?
2639 013374 012637 000004 MOV (SP)+,@ERRVEC ;;RESTORE THE ERROR VECTOR
2640 013400 000463 BR $SVLAD ;;GO TO THE NEXT TEST
2641 013402 022626 5$: CMP (SP)+,(SP)+ ;;CLEAR THE STACK AFTER A TIME OUT
2642 013404 012637 000004 MOV (SP)+,@ERRVEC ;;RESTORE THE ERROR VECTOR
2643 013410 000423 BR 7$ ;;LOOP ON THE PRESENT TEST
2644 013412 6$:;*****END OF CODE FOR THE XOR TESTER*****
2645 013412 032777 000400 165520 BIT @BIT08,@SWR ;;LOOP ON SPEC. TEST?
2646 013420 001404 BEQ 2$ ;;BR IF NO
2647 013422 127737 165512 001102 CMPB @SWR,$STNM ;;ON THE RIGHT TEST? SWR<7:0>
2648 013430 001462 BEQ $OVER ;;BR IF YES
2649 013432 105737 001103 2$: TSTB $ERFLG ;;HAS AN ERROR OCCURRED?
2650 013436 001421 BEQ 3$ ;;BR IF NO
2651 013440 123737 001115 001103 CMPB $ERMAX,$ERFLG ;;MAX. ERRORS FOR THIS TEST OCCURRED?
2652 013446 101015 BHI 3$ ;;BR IF NO
2653 013450 032777 001000 165462 BIT @BIT09,@SWR ;;LOOP ON ERROR?
2654 013456 001404 BEQ 4$ ;;BR IF NO
2655 013460 013737 001110 001106 7$: MOV $LPERR,$LPAOR ;;SET LOOP ADDRESS TO LAST SCOPE
2656 013466 000443 BR $OVER
2657 013470 105037 001103 4$: CLRB $ERFLG ;;ZERO THE ERROR FLAG
2658 013474 005037 001222 CLR $TIMES ;;CLEAR THE NUMBER OF ITERATIONS TO MAKE
2659 013500 000415 BR 1$ ;;ESCAPE TO THE NEXT TEST
2660 013502 032777 004000 165430 3$: BIT @BIT11,@SWR ;;INHIBIT ITERATIONS?

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2661 013510 001011 BNE 1$          ; BR IF YES
2662 013512 005737 001100 TST $PASS      ; IF FIRST PASS OF PROGRAM
2663 013516 001406 BEQ 1$          ; INHIBIT ITERATIONS
2664 013520 005237 001104 INC $ICNT      ; INCREMENT ITERATION COUNT
2665 013524 023737 001222 001104 CMP $TIMES,$ICNT ; CHECK THE NUMBER OF ITERATIONS MADE
2666 013532 002021 BGE $OVER      ; BR IF MORE ITERATION REQUIRED
2667 013534 012737 000001 001104 1$: MOV #1,$ICNT ; REINITIALIZE THE ITERATION COUNTER
2668 013542 013737 013612 001222 MOV $SMXCNT,$TIMES ; SET NUMBER OF ITERATIONS TO DO
2669 013550 105237 001102 $SVLAD: INCB $STNM ; COUNT TEST NUMBERS
2670 013554 011637 001106 MOV ($SP),$LPADR ; SAVE SCOPE LOOP ADDRESS
2671 013560 011637 001110 MOV ($SP),$LPERR ; SAVE ERROR LOOP ADDRESS
2672 013564 005037 001224 CLR $ESCAPE    ; CLEAR THE ESCAPE FROM ERROR ADDRESS
2673 013570 112737 000001 001115 MOVB #1,$ERMAX ; ONLY ALLOW ONE(1) ERROR ON NEXT TEST
2674 013576 013777 001102 165336 $OVER: MOV $STNM,$DISPLAY ; DISPLAY TEST NUMBER
2675 013604 013716 001106 MOV $LPADR,($SP) ; FUDGE RETURN ADDRESS
2676 013610 000002 RTI          ; FIXES PS
2677 013612 000004 $MXCNT: 4          ; MAX. NUMBER OF ITERATIONS
2678 .MACRO SAVE
2679 MOV SP,$REG6
2680 SUB #4,$REG6
2681 MOV 2($SP),$REG7
2682 CLR $REG5
2683 MOVB $STNM,$REG5
2684 MOV @TCM,$REG2
2685 MOV @TCST,$REG1
2686 MOV @TCBA,$REG3
2687 .ENDM SAVE
2688 013614 .ERROR $ERRTYP,SAVE
2689 .SBTTL ERROR HANDLER ROUTINE
2690
2691 013614 STARS
2692 ;*****
2693 ;THIS ROUTINE WILL INCREMENT THE ERROR FLAG AND THE ERROR COUNT,
2694 ;SAVE THE ERROR ITEM NUMBER AND THE ADDRESS OF THE ERROR CALL
2695 ;AND GO TO $ERRTYP ON ERROR
2696 ;THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:
2697 ;$SW15=1 HALT ON ERROR
2698 ;$SW13=1 INHIBIT ERROR TYPEOUTS
2699 ;$SW10=1 BELL ON ERROR
2700 ;$SW09=1 LOOP ON ERROR
2701 ;CALL
2702 ;* ERROR N ;;ERROR=EMT AND N=ERROR ITEM NUMBER
2703
2704 013614 $ERROR:
2705 .IRP NEWINS,<SAVE>
2706 NEWINS
2707 .ENDM
2708 013614 SAVE
2709 013614 010637 001176 MOV SP,$REG6
2710 013620 162737 000004 001176 SUB #4,$REG6
2711 013626 016637 000002 001200 MOV 2($SP),$REG7
2712 013634 005037 001174 CLR $REG5
2713 013640 113737 001102 001174 MOVB $STNM,$REG5
2714 013646 017737 165366 001166 MOV @TCM,$REG2
2715 013654 017737 165356 001164 MOV @TCST,$REG1
2716 013662 017737 165356 001170 MOV @TCBA,$REG3

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2717 013670 105237 001103 7$: INCB SERFLG          ;; SET THE ERROR FLAG
2718 013674 001775          BEQ 7$              ;; DON'T LET THE FLAG GO TO ZERO
2719 013676 013777 001102 165236 MOV STSTNM,DISP     ;; DISPLAY TEST NUMBER AND ERROR FLAG
2720 013704 032777 002000 165226 BIT #BIT10,DSWR    ;; BELL ON ERROR?
2721 013712 001402          BEQ 1$              ;; NO - SKIP
2722 013714 104401 001226          TYPE ,SBELL        ;; RING BELL
2723 013720 005237 001112 15$: INC $ERTTL        ;; COUNT THE NUMBER OF ERRORS
2724 013724 011637 001116          MOV (SP),SERAPC    ;; GET ADDRESS OF ERROR INSTRUCTION
2725 013730 162737 000002 001116 SUB #2,SERAPC
2726 013736 117737 165154 001114 MOVVB #SERAPC,$ITEMB ;; STRIP AND SAVE THE ERROR ITEM CODE
2727 013744 032777 020000 165166 BIT #BIT13,DSWR    ;; SKIP TYPEOUT IF SET
2728 013752 001004          BNE 20$           ;; SKIP TYPEOUTS
2729 013754 004737 015122          JSR PC,SERRTYP    ;; GO TO USER ERROR ROUTINE
2730 013760 104401 001233          TYPE ,SCLF
2731 013764          20$:
2732 013764 005777 165150 2$: TST DSWR          ;; HALT ON ERROR
2733 013770 100001          BPL 3$           ;; SKIP IF CONTINUE
2734 013772 000000          HALT          ;; HALT ON ERROR!
2735 013774 032777 001000 165136 3$: BIT #BIT09,DSWR    ;; LOOP ON ERROR SWITCH SET?
2736 014002 001402          BEQ 4$           ;; BR IF NO
2737 014004 013716 001110          MOV $LPERR,(SP)   ;; FUDGE RETURN FOR LOOPING
2738 014010 005737 001224 4$: TST $ESCAPE        ;; CHECK FOR AN ESCAPE ADDRESS
2739 014014 001402          BEQ 5$           ;; BR IF NONE
2740 014016 013716 001224          MOV $ESCAPE,(SP) ;; FUDGE RETURN ADDRESS FOR ESCAPE
2741 014022          5$:
2742          .LIST
2743 014022 022737 011600 000042 CMP #SENDAD,#42    ;; ACT-11 AUTO-ACCEPT?
2744 014030 001001          BNE 6$           ;; BRANCH IF NO
2745 014032 000000          HALT          ;; YES
2746 014034          6$:
2747 014034 000002          RTI          ;; RETURN
2748 014036          .SPOWER <<POWPUS>,<POWPOP>,<POWMES>>
2749          .SBTTL POWER DOWN AND UP ROUTINES
2750
2751 014036          STARS
2752          ;; *****
2753          :POWER DOWN ROUTINE
2754 014036 012737 014212 000024 SPWRDN: MOV #SILLUP,#PWVVEC ;; SET FOR FAST UP
2755 014044 012737 000340 000026 MOV #340,#PWVVEC+2 ;; PRIO:7
2756 014052          PUSH <R0,R1,R2,R3,R4,R5>
2757          .IRP B,<R0,R1,R2,R3,R4,R5>
2758          MOV B,-(SP) ;; PUSH B ON STACK
2759          .ENDM
2760 014052 010046          MOV R0,-(SP) ;; PUSH R0 ON STACK
2761 014054 010146          MOV R1,-(SP) ;; PUSH R1 ON STACK
2762 014056 010246          MOV R2,-(SP) ;; PUSH R2 ON STACK
2763 014060 010346          MOV R3,-(SP) ;; PUSH R3 ON STACK
2764 014062 010446          MOV R4,-(SP) ;; PUSH R4 ON STACK
2765 014064 010546          MOV R5,-(SP) ;; PUSH R5 ON STACK
2766 014066          PUSH <<POWPUS>,<POWPOP>,<POWMES>>
2767          .IRP B,<<POWPUS>,<POWPOP>,<POWMES>>
2768          MOV B,-(SP) ;; PUSH B ON STACK
2769          .ENDM
2770 014066 013746 001312          MOV POWPUS,-(SP) ;; PUSH POWPUS ON STACK
2771 014072 013746 001314          MOV POWPOP,-(SP) ;; PUSH POWPOP ON STACK
2772 014076 013746 016050          MOV POWMES,-(SP) ;; PUSH POWMES ON STACK
    
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2773 014102          .IRP   PUSH   @SWR
2774          .IRP   B (&SWR)
2775          .IRP   MOV   B, -(SP)          ;; PUSH B ON STACK
2776          .ENDM
2777 014102 017746 165032          MOV   @SWR, -(SP)          ;; PUSH @SWR ON STACK
2778 014106 010637 014216          MOV   SP, $SAVR6          ;; SAVE SP
2779 014112 012737 014124 000024  MOV   @SPWRUP, @PWRVEC    ;; SET UP VECTOR
2780 014120 000000          HALT
2781 014122 000776          BR   .-2          ;; HANG UP
2782
2783 014124          STARS
2784          ;*****
2785          :POWER UP ROUTINE
2786 014124 012737 014212 000024 $PWRUP: MOV   @SILLUP, @PWRVEC    ;; SET FOR FAST DOWN
2787 014132 013706 014216          MOV   $$SAVR6, SP          ;; GET SP
2788 014136 005037 014216          CLR   $$SAVR6          ;; WAIT LOOP FOR THE TTY
2789 014142 005237 014216 1$: INC   $$SAVR6          ;; WAIT FOR THE INC
2790 014146 001375          BNE   1$          ;; OF <POWPUS>, <POWPOP>, <POWMES> WORD
2791 014150          POP   @SWR
2792          .IRP   B (&SWR)
2793          .IRP   MOV   (SP)+, B          ;; POP STACK INTO B
2794          .ENDM
2795 014150 012677 164764          MOV   (SP)+, @SWR          ;; POP STACK INTO @SWR
2796 014154          POP   <R5, R4, R3, R2, R1, R0>
2797          .IRP   B (&R5, R4, R3, R2, R1, R0)
2798          .IRP   MOV   (SP)+, B          ;; POP STACK INTO B
2799          .ENDM
2800 014154 012605          MOV   (SP)+, R5          ;; POP STACK INTO R5
2801 014156 012604          MOV   (SP)+, R4          ;; POP STACK INTO R4
2802 014160 012603          MOV   (SP)+, R3          ;; POP STACK INTO R3
2803 014162 012602          MOV   (SP)+, R2          ;; POP STACK INTO R2
2804 014164 012601          MOV   (SP)+, R1          ;; POP STACK INTO R1
2805 014166 012600          MOV   (SP)+, R0          ;; POP STACK INTO R0
2806 014170 012737 014036 000024  MOV   @SPWRON, @PWRVEC    ;; SET UP THE POWER DOWN VECTOR
2807 014176 012737 000340 000026  MOV   @340, @PWRVEC+2    ;; Prio:7
2808 014204 104401          TYPE          ;; REPORT THE POWER FAILURE
2809 014206 014220 $PWRMG: .WORD  $POWER          ;; POWER FAIL MESSAGE POINTER
2810 014210 000002          RTI
2811 014212 000000 $SILLUP: HALT          ;; THE POWER UP SEQUENCE WAS STARTED
2812 014214 000776          BR   .-2          ;; BEFORE THE POWER DOWN WAS COMPLETE
2813 014216 000000 $SAVR6: 0          ;; PUT THE SP HERE
2814 014220 005015 047520 042527 $POWER: .ASCIZ <15><12>"POWER"
2815 014226 000122          .EVEN
2816
2817 014230          .$TYPE
2818          .SBTTL TYPE ROUTINE
2819
2820 014230          STARS
2821          ;*****
2822          :ROUTINE TO TYPE ASCIZ MESSAGE. MESSAGE MUST TERMINATE WITH A 0 BYTE.
2823          :THE ROUTINE WILL INSERT A NUMBER OF NULL CHARACTERS AFTER A LINE FEED.
2824          :*NOTE1: $NULL CONTAINS THE CHARACTER TO BE USED AS THE FILLER CHARACTER.
2825          :*NOTE2: $FILLS CONTAINS THE NUMBER OF FILLER CHARACTERS REQUIRED.
2826          :*NOTE3: $FILLC CONTAINS THE CHARACTER TO FILL AFTER.
2827          :*
2828          :*CALL:

```

```

2829 ;*1) USING A TRAP INSTRUCTION
2830 ;* TYPE ,MESADR ;;MESADR IS FIRST ADDRESS OF AN ASCIZ STRING
2831 ;*OR
2832 ;* TYPE
2833 ;* MESADR
2834 ;*
2835
2836 $TYPE: TSTB STPFLG ;; IS THERE A TERMINAL?
2837 BPL 1$ BR IF YES
2838 HALT 000000 HALT HERE IF NO TERMINAL
2839 BR 3$ LEAVE
2840 1$: MOV RO,-(SP) SAVE RO
2841 MOV 22(SP),RO GET ADDRESS OF ASCIZ STRING
2842 2$: MOVB (RO)+,-(SP) PUSH CHARACTER TO BE TYPED ONTO STACK
2843 BNE 4$ BR IF IT ISN'T THE TERMINATOR
2844 TST (SP)+ IF TERMINATOR POP IT OFF THE STACK
2845 60$: MOV (SP)+,RO RESTORE RO
2846 3$: ADD #2,(SP) ADJUST RETURN PC
2847 RTI RETURN
2848 4$: CMPB #HT,(SP) BRANCH IF <HT>
2849 BEQ 8$
2850 CMPB #CRLF,(SP) ;; BRANCH IF NOT <CRLF>
2851 BNE 5$
2852 TST (SP)+ ;; POP <CR><LF> EQUIV
2853 TYPE TYPE A CR AND LF
2854 SCRLF
2855 CLRFB $CHARCNT ;; CLEAR CHARACTER COUNT
2856 BR 2$ GET NEXT CHARACTER
2857 5$: JSR PC,$TYPEC GO TYPE THIS CHARACTER
2858 6$: CMPB $FILLC,(SP)+ IS IT TIME FOR FILLER CHARS.?
2859 BNE 2$ IF NO GO GET NEXT CHAR.
2860 MOV $NULL,-(SP) GET # OF FILLER CHARS. NEEDED
2861 AND THE NULL CHAR.
2862 7$: DECB 1(SP) DOES A NULL NEED TO BE TYPED?
2863 BLT 6$ BR IF NO--GO POP THE NULL OFF OF STACK
2864 JSR PC,$TYPEC GO TYPE A NULL
2865 DECB $CHARCNT DO NOT COUNT AS A COUNT
2866 BR 7$ LOOP
2867
2868 ;HORIZONTAL TAB PROCESSOR
2869
2870 8$: MOVB #' (SP) REPLACE TAB WITH SPACE
2871 9$: JSR PC,$TYPEC TYPE A SPACE
2872 BITB #7,$CHARCNT BRANCH IF NOT AT
2873 BNE 9$ TAB STOP
2874 TST (SP)+ POP SPACE OFF STACK
2875 BR 2$ GET NEXT CHARACTER
2876 $TYPEC: TSTB 2STPS WAIT UNTIL PRINTER IS READY
2877 BPL $TYPEC
2878 MOVB 2(SP),2STPB ;; LOAD CHAR TO BE TYPED INTO DATA REG.
2879 CMPB #CR,2(SP) IS CHARACTER A CARRIAGE RETURN?
2880 BNE 1$ BRANCH IF NO
2881 CLRFB $CHARCNT YES--CLEAR CHARACTER COUNT
2882 BR $TYPEX EXIT
2883 1$: CMPB #LF,2(SP) IS CHARACTER A LINE FEED?
2884 BEQ $TYPEX BRANCH IF YES

```

2885 014442 105227  
2886 014444 000000  
2887 014446 000207  
2888  
2889 014450  
2890  
2891  
2892 014450  
2893  
2894  
2895  
2896  
2897  
2898  
2899  
2900  
2901  
2902  
2903 014450  
2904  
2905  
2906  
2907 014450 010046  
2908 014452 010146  
2909 014454 010246  
2910 014456 010346  
2911 014460 010546  
2912 014462 012746 020200  
2913 014466 016605 000020  
2914 014472 100004  
2915 014474 005405  
2916 014476 112756 000055 000001  
2917 014504 005000 15:  
2918 014506 012703 014664  
2919 014512 112723 000040  
2920 014516 005002 25:  
2921 014520 016001 014654  
2922 014524 160105 35:  
2923 014526 002402  
2924 014530 005202  
2925 014532 000774  
2926 014534 060105 45:  
2927 014536 005702  
2928 014540 001002  
2929 014542 105716  
2930 014544 100407  
2931 014546 106316 55:  
2932 014550 103003  
2933 014552 116663 000001 177777  
2934 014560 052702 000060  
2935 014564 052702 000040  
2936 014570 110223  
2937 014572 005720  
2938 014574 020027 000010  
2939 014600 002746  
2940 014602 003002

```
INCB (PC)+ ;;COUNT THE CHARACTER
$CHARCNT: WORD 0 ;;CHARACTER COUNT STORAGE
$TYPEX: RTS PC

.$STYPDEC
.$SBTTL CONVERT BINARY TO DECIMAL AND TYPE ROUTINE

STARS
:*****
:THIS ROUTINE IS USED TO CHANGE A 16-BIT BINARY NUMBER TO A 5-DIGIT
: SIGNED DECIMAL (ASCII) NUMBER AND TYPE IT. DEPENDING ON WHETHER THE
: NUMBER IS POSITIVE OR NEGATIVE A SPACE OR A MINUS SIGN WILL BE TYPED
: BEFORE THE FIRST DIGIT OF THE NUMBER. LEADING ZEROS WILL ALWAYS BE
: REPLACED WITH SPACES.
:CALL:
:* MOV NUM,-(SP) ;;PUT THE BINARY NUMBER ON THE STACK
:* TYPDS ;;GO TO THE ROUTINE

$TYPDS: PUSH (R0,R1,R2,R3,R5)
.IRP B,(R0,R1,R2,R3,R5)
MOV B,-(SP) ;;PUSH B ON STACK
.ENDM

MOV R0,-(SP) ;;PUSH R0 ON STACK
MOV R1,-(SP) ;;PUSH R1 ON STACK
MOV R2,-(SP) ;;PUSH R2 ON STACK
MOV R3,-(SP) ;;PUSH R3 ON STACK
MOV R5,-(SP) ;;PUSH R5 ON STACK
MOV #20200,-(SP) ;;SET BLANK SWITCH AND SIGN
MOV 20(SP),R5 ;;GET THE INPUT NUMBER
BPL 1$ ;;BR IF INPUT IS POS.
NEG R5 ;;MAKE THE BINARY NUMBER POS.
MOVB #'-',1(SP) ;;MAKE THE ASCII NUMBER NEG.
1$: CLR R0 ;;ZERO THE CONSTANTS INDEX
MOV #508LK,R3 ;;SETUP THE OUTPUT POINTER
MOVB #'',(R3)+ ;;SET THE FIRST CHARACTER TO A BLANK
2$: CLR R2 ;;CLEAR THE BCD NUMBER
MOV $DTBL(R0),R1 ;;GET THE CONSTANT
SUB R1,R5 ;;FORM THIS BCD DIGIT
BLT 4$ ;;BR IF DONE
INC R2 ;;INCREASE THE BCD DIGIT BY 1
BR 3$
3$: BR R1,R5 ;;ADD BACK THE CONSTANT
4$: TST R2 ;;CHECK IF BCD DIGIT=0
BNE 5$ ;;FALL THROUGH IF 0
TSTB (SP) ;;STILL DOING LEADING 0'S?
BMI 7$ ;;BR IF YES
5$: ASLB (SP) ;;MSD?
BCC 6$ ;;BR IF NO
MOVB 1(SP),-1(R3) ;;YES--SET THE SIGN
6$: BIS #'0,R2 ;;MAKE THE BCD DIGIT ASCII
7$: BIS #' ,R2 ;;MAKE IT A SPACE IF NOT ALREADY A DIGIT
MOVB R2,(R3)+ ;;PUT THIS CHARACTER IN THE OUTPUT BUFFER
TST (R0)+ ;;JUST INCREMENTING
CMP R0,#10 ;;CHECK THE TABLE INDEX
BLT 2$ ;;GO DO THE NEXT DIGIT
BGT 8$ ;;GO TO EXIT
```

K05

MAINDEC-11-DZTCB-D TC11 TEST #2  
 DZTCB0.P11 18-FEB-77 10:59

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 CONVERT BINARY TO DECIMAL AND TYPE ROUTINE

2941	014604	010502			MOV	R5,R2	:: GET THE LSD
2942	014606	000764			BR	6\$	:: GO CHANGE TO ASCII
2943	014610	105726			BS:	TSTB (SP)+	:: WAS THE LSD THE FIRST NON-ZERO?
2944	014612	100003				BPL 9\$	:: BR IF NO
2945	014614	116663	177777	177776	9\$:	MOVW -1(SP),-2(R3)	:: YES--SET THE SIGN FOR TYPING
2946	014622	105013				CLRB (R3)	:: SET THE TERMINATOR
2947	014624					POP <R5,R3,R2,R1,R0>	
2948					.IRP	B,<R5,R3,R2,R1,R0>	
2949						MOV (SP)+,B	:: POP STACK INTO B
2950					.ENDM		
2951	014624	012605				MOV (SP)+,R5	:: POP STACK INTO R5
2952	014626	012603				MOV (SP)+,R3	:: POP STACK INTO R3
2953	014630	012602				MOV (SP)+,R2	:: POP STACK INTO R2
2954	014632	012601				MOV (SP)+,R1	:: POP STACK INTO R1
2955	014634	012600				MOV (SP)+,R0	:: POP STACK INTO R0
2956	014636	104401	014664			TYPE \$DBLK	:: NOW TYPE THE NUMBER
2957	014642	016666	000002	000004		MOV 2(SP),4(SP)	:: ADJUST THE STACK
2958	014650	012616				MOV (SP)+,(SP)	
2959	014652	000002				RTI	:: RETURN TO USER
2960	014654	023420			\$DTBL:	10000.	
2961	014656	001750				1000.	
2962	014660	000144				100.	
2963	014662	000012				10.	
2964	014664	000004			\$DBLK:	.BLKW 4	
2965	014674				.STYPOCT		
2966					.SBTTL	BINARY TO OCTAL (ASCII) AND TYPE	
2967					STARS		
2968	014674				:: *****		
2969					:: *THIS ROUTINE IS USED TO CHANGE A 16-BIT BINARY NUMBER TO A 6-DIGIT		
2970					:: *OCTAL (ASCII) NUMBER AND TYPE IT.		
2971					:: *STYPOS---ENTER HERE TO SETUP SUPPRESS ZEROS AND NUMBER OF DIGITS TO TYPE		
2972					:: *CALL:		
2973					:: * MOV NUM,-(SP) :: NUMBER TO BE TYPED		
2974					:: * TYPOS :: CALL FOR TYPEOUT		
2975					:: * .BYTE N :: N=1 TO 6 FOR NUMBER OF DIGITS TO TYPE		
2976					:: * .BYTE M :: M=1 OR 0		
2977					:: * :: I=TYPE LEADING ZEROS		
2978					:: * :: O=SUPPRESS LEADING ZEROS		
2979					:: * *STYPON---ENTER HERE TO TYPE OUT WITH THE SAME PARAMETERS AS THE LAST		
2980					:: * *STYPOS OR STYPOC		
2981					:: * *CALL:		
2982					:: * MOV NUM,-(SP) :: NUMBER TO BE TYPED		
2983					:: * TYPON :: CALL FOR TYPEOUT		
2984					:: * *STYPOC---ENTER HERE FOR TYPEOUT OF A 16 BIT NUMBER		
2985					:: * *CALL:		
2986					:: * MOV NUM,-(SP) :: NUMBER TO BE TYPED		
2987					:: * TYPOC :: CALL FOR TYPEOUT		
2988					:: * *STYPOS: MOV 2(SP),-(SP) :: PICKUP THE MODE		
2989					:: * MOVW 1(SP),\$OFILL :: LOAD ZERO FILL SWITCH		
2990					:: * MCVB (SP)+,\$OMODE+1 :: NUMBER OF DIGITS TO TYPE		
2991					:: * ADD #2,(SP) :: ADJUST RETURN ADDRESS		
2992	014674	017646	000000			BR \$TYPON	
2993	014700	116637	000001	015117			
2994	014706	112637	015121				
2995	014712	062716	000002				
2996	014716	000406					

```

2997 014720 112737 000001 015117 $TYPOC: MOVB #1,$OFILL      ;; SET THE ZERO FILL SWITCH
2998 014726 112737 000006 015121      MOVB #6,$SOMODE+1    ;; SET FOR SIX(6) DIGITS
2999 014734 112737 000005 015116 $TYPON: MOVB #5,$SOCNT  ;; SET THE ITERATION COUNT
3000 014742 010346      MOV R3,-(SP)        ;; SAVE R3
3001 014744 010446      MOV R4,-(SP)        ;; SAVE R4
3002 014746 010546      MOV R5,-(SP)        ;; SAVE R5
3003 014750 113704 015121      MOVB $SOMODE+1,R4   ;; GET THE NUMBER OF DIGITS TO TYPE
3004 014754 005404      NEG R4              ;;
3005 014756 062704 000006      ADD #6,R4           ;; SUBTRACT IT FOR MAX. ALLOWED
3006 014762 110437 015120      MOVB R4,$SOMODE     ;; SAVE IT FOR USE
3007 014766 113704 015117      MOVB $OFILL,R4      ;; GET THE ZERO FILL SWITCH
3008 014772 016605 000012      MOV 12(SP),R5       ;; PICKUP THE INPUT NUMBER
3009 014776 005003      CLR R3              ;; CLEAR THE OUTPUT WORD
3010 015000 006105      1$: ROL R5          ;; ROTATE MSB INTO "C"
3011 015002 000404      BR 3$               ;; GO DO MSB
3012 015004 006105      2$: ROL R5          ;; FORM THIS DIGIT
3013 015006 006105      ROL R5
3014 015010 006105      ROL R5
3015 015012 010503      MOV R5,R3           ;;
3016 015014 006103      3$: ROL R3           ;; GET LSB OF THIS DIGIT
3017 015016 105337 015120      DECB $SOMODE         ;; TYPE THIS DIGIT?
3018 015022 100016      BPL 7$              ;; BR IF NO
3019 015024 042703 177770      BIC #177770,R3      ;; GET RID OF JUNK
3020 015030 001002      BNE 4$              ;; TEST FOR 0
3021 015032 005704      TST R4              ;; SUPPRESS THIS 0?
3022 015034 001403      BEQ 5$              ;; BR IF YES
3023 015036 005204      4$: INC R4           ;; DON'T SUPPRESS ANYMORE 0'S
3024 015040 052703 000060      BIS #'0,R3          ;; MAKE THIS DIGIT ASCII
3025 015044 052703 000040      5$: BIS #' ,R3       ;; MAKE ASCII IF NOT ALREADY
3026 015050 110337 015114      MOVB R3,$S          ;; SAVE FOR TYPING
3027 015054 104401 015114      TYPE #8$            ;; GO TYPE THIS DIGIT
3028 015060 105337 015116      7$: DECB $SOCNT      ;; COUNT BY 1
3029 015064 003347      BGT 2$              ;; BR IF MORE TO DO
3030 015066 002402      BLT 6$              ;; BR IF DONE
3031 015070 005204      INC R4              ;; INSURE LAST DIGIT ISN'T A BLANK
3032 015072 000744      BR 2$               ;; GO DO THE LAST DIGIT
3033 015074 012605      6$: MOV (SP)+,R5      ;; RESTORE R5
3034 015076 012604      MOV (SP)+,R4        ;; RESTORE R4
3035 015100 012603      MOV (SP)+,R3        ;; RESTORE R3
3036 015102 016666 000002 000004      MOV 2(SP),4(SP)     ;; SET THE STACK FOR RETURNING
3037 015110 012616      MOV (SP)+,(SP)     ;;
3038 015112 000002      RTI                 ;; RETURN
3039 015114 000      8$: .BYTE 0         ;; STORAGE FOR ASCII DIGIT
3040 015115 000      .BYTE 0           ;; TERMINATOR FOR TYPE ROUTINE
3041 015116 000      $SOCNT: .BYTE 0   ;; OCTAL DIGIT COUNTER
3042 015117 000      $OFILL: .BYTE 0   ;; ZERO FILL SWITCH
3043 015120 000000      $SOMODE: .WORD 0  ;; NUMBER OF DIGITS TO TYPE
3044 015122      .SERRTYP
3045      .SBTTL ERROR MESSAGE TYPEOUT ROUTINE
3046
3047 015122      STARS
3048      ;*****
3049      ;THIS ROUTINE USES THE "ITEM CONTROL BYTE" ($ITEMB) TO DETERMINE WHICH
3050      ;*ERROR IS TO BE REPORTED. IT THEN OBTAINS, FROM THE "ERROR TABLE" ($ERRTB),
3051      ;*AND REPORTS THE APPROPRIATE INFORMATION CONCERNING THE ERROR.
3052

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3053 015122
3054 015122 104401 001233
3055 015126 010046
3056 015130 005000
3057 015132 153700 001114
3058 015136 001004
3059
3060 015140
3061 015140 013746 001116
3062
3063 015144 104402
3064 015146 000426
3065 015150 005300
3066 015152 006300
3067 015154 006300
3068 015156 006300
3069 015160 062700 001322
3070 015164 012037 015174
3071 015170 001404
3072 015172 104401
3073 015174 000000
3074 015176 104401 001233
3075 015202 012037 015212
3076 015206 001404
3077 015210 104401
3078 015212 000000
3079 015214 104401 001233
3080 015220 011000
3081 015222 001004
3082 015224 012600
3083 015226 104401 001233
3084 015232 000207
3085 015234
3086 015234 013046
3087 015236 104402
3088 015240 005710
3089 015242 001770
3090 015244 104401 015252
3091 015250 000771
3092 015252 020040 000
3093 015256
3094 015256
3095
3096
3097 015256
3098
3099
3100
3101
3102
3103
3104 015256 010046
3105 015260 116600 000002
3106 015264 005740
3107 015266 111000
3108 015270 006300

```

```

SERRTYP:
TYPE          $CRLF          ;; "CARRIAGE RETURN" & "LINE FEED"
MOV          RO,-(SP)        ;; SAVE RO
CLR          RO              ;; PICKUP THE ITEM INDEX
BISB        2($ITEMB,RO)
BNE          1$              ;; IF ITEM NUMBER IS ZERO, JUST
                           ;; TYPE THE PC OF THE ERROR
TYPOCT      $ERRPC,(ERROR ADDRESS)
MOV          $ERRPC,-(SP)    ;; SAVE $ERRPC FOR TIMEOUT
                           ;; ERROR ADDRESS
                           ;; GO TYPE--OCTAL ASCII(ALL DIGITS)
                           ;; GET OUT
                           ;; ADJUST THE INDEX SO THAT IT WILL
                           ;; WORK FOR THE ERROR TABLE
1$:          BR              6$
DEC          RO
ASL          RO
ASL          RO
ASL          RO
ADD          $ERRTB,RO      ;; FORM TABLE POINTER
MOV          (RO)+,2$      ;; PICKUP "ERROR MESSAGE" POINTER
BEQ          3$            ;; SKIP TIMEOUT IF NO POINTER
TYPE        $CRLF          ;; TYPE THE "ERROR MESSAGE"
WORD        0              ;; "E" OR "MES" "E" POINTER GOES HERE
2$:          TYPE          $CRLF  ;; "CARRIAGE RETURN" & "LINE FEED"
MOV          (RO)+,4$      ;; PICKUP "DATA HEADER" POINTER
BEQ          5$            ;; SKIP TIMEOUT IF 0
TYPE        $CRLF          ;; TYPE THE "DATA HEADER"
WORD        0              ;; "DATA HEADER" POINTER GOES HERE
3$:          TYPE          $CRLF  ;; "CARRIAGE RETURN" & "LINE FEED"
MOV          (RO),RO      ;; PICKUP "DATA TABLE" POINTER
BNE          7$            ;; GO TYPE THE DATA
MOV          (SP)+,RO      ;; RESTORE RO
TYPE        $CRLF          ;; "CARRIAGE RETURN" & "LINE FEED"
RTS          PC            ;; RETURN
7$:          TYPOCT      2(RO)+  ;; TYPE AN OCTAL NUMBER
MOV          2(RO)+,-(SP)  ;; SAVE 2(RO)+ FOR TIMEOUT
TYPOCT      $CRLF          ;; GO TYPE--OCTAL ASCII(ALL DIGITS)
TST         (RO)          ;; IS THERE ANOTHER NUMBER?
BEQ          6$            ;; BR IF NO
TYPE        8$            ;; TYPE TWO(2) SPACES
BR          7$            ;; LOOP
8$:          .ASCIZ      / /  ;; TWO(2) SPACES
        .EVEN
        .STRAP
        .SBTTL TRAP DECODER

STARS
*****
*THIS ROUTINE WILL PICKUP THE LOWER BYTE OF THE "TRAP" INSTRUCTION
*AND USE IT TO INDEX THROUGH THE TRAP TABLE FOR THE STARTING ADDRESS
*OF THE DESIRED ROUTINE. THEN USING THE ADDRESS OBTAINED IT WILL
*GO TO THAT ROUTINE.

$TRAP:      MOV          RO,-(SP)  ;; SAVE RO
MOV          2(SP),RO      ;; GET TRAP ADDRESS
TST         -(RO)         ;; BACKUP BY 2
MOVB        (RO),RO      ;; GET RIGHT BYTE OF TRAP
ASL         RO            ;; POSITION FOR INDEXING

```

```

3109 015272 016000 015312          MOV  $TRPAD(RO),RO  ;;INDEX TO TABLE
3110 015276 000200                RTS  RO              ;;GO TO ROUTINE
3111
3112
3113          ;;THIS IS USE TO HANDLE THE "GETPRI" MACRO
3114
3115 015300 011646                $TRAP2: MOV  (SP),-(SP)  ;;MOVE THE PC DOWN
3116 015302 016666 000004 000002  MOV  4(SP),2(SP)    ;;MOVE THE PSW DOWN
3117 015310 000002                RTI                    ;;RESTORE THE PSW
3118
3119          .MACRO  SETTRAP A,B,MSG
3120          $$SET  A,B,\<TRAP+$TRP>,\$TRP,<MSG>
3121          .NLIST
3122          $TRP=$TRP+1
3123          .LIST
3124          .ENDM  SETTRAP
3125          .MACRO  $$SET  A,B,C,D,COMNT
3126          .IF EQ $TRP-1
3127          .SBTTL  TRAP TABLE
3128
3129          ;*THIS TABLE CONTAINS THE STARTING ADDRESSES OF THE ROUTINES CALLED
3130          ;*BY THE "TRAP" INSTRUCTION.
3131
3132          ;          ROUTINE
3133          ;          -----
3134          $TRPAD: .WORD  $TRAP2
3135          .ENDC
3136          .IIF NDF GNS,.NLIST
3137          A= C
3138          .IIF NDF GNS,.LIST
3139          B          ;;CALL=A          TRAP+D(C)          COMNT
3140          .ENDM  $$SET
3141          .MACRO  TRMTRP
3142          $TERM=-$TRPAD
3143          .ENDM  TRMTRP
3144          .LIST
3145 015312          SETTRAP TYPE,$TYPE,↑/TTY TYPEOUT ROUTINE/
3146 015312          $$SET  TYPE,$TYPE,\<TRAP+$TRP>,\$TRP,<TTY TYPEOUT ROUTINE>
3147          .SBTTL  TRAP TABLE
3148
3149          ;*THIS TABLE CONTAINS THE STARTING ADDRESSES OF THE ROUTINES CALLED
3150          ;*BY THE "TRAP" INSTRUCTION.
3151
3152          ;          ROUTINE
3153          ;          -----
3154 015312 015300          $TRPAD: .WORD  $TRAP2
3155          .LIST
3156 015314 014230          $TYPE  ;;CALL=TYPE          TRAP+1(104401)  TTY TYPEOUT ROUTINE
3157          .LIST
3158 015316          SETTRAP TYPOC,$TYPOC,↑/TYPE OCTAL NUMBER (WITH LEADING ZEROS)/
3159 015316          $$SET  TYPOC,$TYPOC,\<TRAP+$TRP>,\$TRP,<TYPE OCTAL NUMBER (WITH LEADING ZEROS)>
3160          .LIST
3161 015316 014720          $TYPOC  ;;CALL=TYPOC          TRAP+2(104402)  TYPE OCTAL NUMBER (WITH LEADING ZEROS)
3162          .LIST
3163 015320          SETTRAP TYPOS,$TYPOS,↑/TYPE OCTAL NUMBER (NO LEADING ZEROS)/
3164 015320          $$SET  TYPOS,$TYPOS,\<TRAP+$TRP>,\$TRP,<TYPE OCTAL NUMBER (NO LEADING ZEROS)>
    
```

3165					.LIST	
3166	015320	014674			\$TYPOS ;;CALL=TYPOS TRAP+3(104403) TYPE OCTAL NUMBER (NO LEADING ZEROS)	
3167					.LIST	
3168	015322				SETTRAP TYPON,\$TYPON,↑/TYPE OCTAL NUMBER (AS PER LAST CALL)/	
3169	015322				\$\$SET TYPON,\$TYPON,\<TRAP+\$TRP>,\STRP,<TYPE OCTAL NUMBER (AS PER LAST CALL)>	
3170					.LIST	
3171	015322	014734			\$TYPON ;;CALL=TYPON TRAP+4(104404) TYPE OCTAL NUMBER (AS PER LAST CALL)	
3172					.LIST	
3173	015324				SETTRAP TYPDS,\$TYPDS,↑/TYPE DECIMAL NUMBER (WITH SIGN)/	
3174	015324				\$\$SET TYPDS,\$TYPDS,\<TRAP+\$TRP>,\STRP,<TYPE DECIMAL NUMBER (WITH SIGN)>	
3175					.LIST	
3176	015324	014450			\$TYPDS ;;CALL=TYPDS TRAP+5(104405) TYPE DECIMAL NUMBER (WITH SIGN)	
3177					.LIST	
3178						
3179						
3180	015326	000000			CKSELT: OPEN	
3181	015330	055104	041524	026502	STMES: .ASCII 'DZTCB-D - TC11 TEST'<15><12>	
3182	015336	020104	020055	041524		
3183	015344	030461	052040	051505		
3184	015352	006524	012			
3185	015355	123	052105	052440	.ASCII 'SET UNITS TO REMOTE AND WRITE LOCK.'	
3186	015362	044516	030124	052040		
3187	015370	020117	042522	047515		
3188	015376	042524	040740	042116		
3189	015404	053440	044522	042524		
3190	015412	046040	041517	027113		
3191	015420	046101	020114	052117	.ASCII 'ALL OTHER UNITS OFF.'<15><12>	
3192	015426	042510	020122	047125		
3193	015434	052111	020123	043117		
3194	015442	027106	005015			
3195	015446	051127	046524	051440	.ASCIIZ 'WRTM SWITCH OFF, WALL SWITCH ON.'<15><12>	
3196	015454	044527	041524	020110		
3197	015462	043117	026106	053440		
3198	015470	046101	020114	053523		
3199	015476	052111	044103	047440		
3200	015504	027116	005015	000		
3201	015511	015	051412	052105	ASETSR: .ASCIIZ <15><12>'SET SR OPTIONS. NORMAL SR = 0'	
3202	015516	051440	020122	050117		
3203	015524	044524	047117	027123		
3204	015532	047040	051117	040515		
3205	015540	020114	051123	036440		
3206	015546	030040	000			
3207	015551	015	044412	053116	AINCRT: .ASCIIZ <15><12>'INVALID TEST.'	
3208	015556	046101	042111	052040		
3209	015564	051505	027124	000		
3210	015571	007			APGEND: .BYTE 007	
3211	015572	025045	000		.ASCIIZ 'X*'	
3212	015575	106	052101	046101	TRPM4S: .ASCIIZ "FATAL ERROR TRAP TO LOCATION 4 FROM LOC"	
3213	015602	042440	051122	051117		
3214	015610	052040	040522	020120		
3215	015616	047524	046040	041517		
3216	015624	052101	047511	020116		
3217	015632	020064	051106	046517		
3218	015640	046040	041517	000		
3219	015645	050	041077	042101	TRPMES: .ASCIIZ "(?BAD CPU?) ATTEMPTING TO RESTART PROGRAM"	
3220	015652	041440	052520	024477		

3221	015660	040440	052124	046505
3222	015666	052120	047111	020107
3223	015674	047524	051040	051505
3224	015702	040424	052122	050040
3225	015710	047522	051107	046501
3226	015716	000		
3227	015717	106	052101	046101
3228	015724	042440	051122	051117
3229	015732	052040	040522	020120
3230	015740	047524	046040	041517
3231	015746	052101	047511	020116
3232	015754	030061	043046	047522
3233	015762	020115	047514	020103
3234	015770	000		
3235	015771	124	051505	051524
3236	015776	040440	042522	047140
3237	016004	052125	047440	020106
3238	016012	042523	052521	047105
3239	016020	042503	026440	026440
3240	016026	026440	051040	051505
3241	016034	040524	052122	047111
3242	016042	027107	027056	000056
3243	016050	005015	042522	052123
3244	016056	051101	044524	043516
3245	016064	040440	052106	051105
3246	016072	040440	050040	053517
3247	016100	051105	043040	044501
3248	016106	052514	042522	005015
3249	016114	000		
3250	016115	123	052101	024040
3251	016122	052123	050117	040440
3252	016130	046114	052040	040522
3253	016136	051516	047520	052122
3254	016144	024523	041440	046517
3255	016152	040515	042116	042040
3256	016160	042111	047040	052117
3257	016166	041440	042514	051101
3258	016174	051040	040505	054504
3259	016202	000		
3260	016203	040	050040	020103
3261	016210	020040	020040	051440
3262	016216	020120	020040	020040
3263	016224	050040	020123	020040
3264	016232	020040	042524	052123
3265	016240	020043	020040	041524
3266	016246	046503	020040	020040
3267	016254	041524	052123	000
3268		016262		
3269	016262	001116	001176	001200
3270	016270	001174	001166	001164
3271	016276	000000		
3272				
3273				
3274	016300	051523	020124	051450
3275	016306	047524	020120	042523
3276	016314	042514	052103	042105

TRPM10: .ASCIZ "FATAL ERROR TRAP TO LOCATION 10 FROM LOC "

RESTART: .ASCIZ "TESTS ARE OUT OF SEQUENCE - - - RESTARTING...."

POWRES: .ASCIZ <15> <12> "RESTARTING AFTER A POWER FAILURE"<15> <12>

EM1: .ASCIZ "SAT (STOP ALL TRANSPORTS) COMMAND DID NOT CLEAR READY"

EM1: .ASCIZ " PC SP PS TEST# TCCM TCST"

.EVEN  
ET1: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1  
000000

EM2: .ASCIZ "SST (STOP SELECTED TRANSPORT) DID NOT CLEAR READY"

MAINDEC-11-DZTCB-D  
DZTCB0.P11

TC11 TEST #2  
18-FEB-77 10:59

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TRAP TABLE

3277	016322	052040	040522	051516
3278	016330	047520	052122	020051
3279	016336	044504	020104	047516
3280	016344	020124	046103	040505
3281	016352	020122	042522	042101
3282	016360	000131		
3283	016362	020040	041520	020040
3284	016370	020040	020040	050123
3285	016376	020040	020040	020040
3286	016404	051520	020040	020040
3287	016412	052040	051505	021524
3288	016420	020040	052040	041503
3289	016426	020115	020040	052040
3290	016434	051503	000124	
3291				
3292	016440	001116	001176	001200
3293	016446	001174	001166	001164
3294	016454	000000		
3295				
3296				
3297	016456	042522	042101	020131
3298	016464	044502	020124	044504
3299	016472	020104	047516	020124
3300	016500	040503	051525	020105
3301	016506	047101	044440	052116
3302	016514	051105	052522	052120
3303	016522	000		
3304	016523	040	050040	020103
3305	016530	020040	020040	051440
3306	016536	020120	020040	020040
3307	016544	050040	020123	020040
3308	016552	020040	042524	052123
3309	016560	020043	020040	041524
3310	016566	046503	020040	020040
3311	016574	041524	052123	000
3312		016602		
3313	016602	001116	001176	001200
3314	016610	001174	001166	001164
3315	016616	000000		
3316				
3317				
3318	016620	042522	042101	020131
3319	016626	044502	020124	040503
3320	016634	051525	042105	040440
3321	016642	020116	047111	042524
3322	016650	051122	050125	020124
3323	016656	044527	044124	050040
3324	016664	047522	042503	051523
3325	016672	051117	040440	042116
3326	016700	052040	030503	020061
3327	016706	052101	051440	046501
3328	016714	020105	051120	047511
3329	016722	044522	054524	000
3330	016727	040	050040	020103
3331	016734	020040	020040	051440
3332	016742	020120	020040	020040

EH2: .ASCIZ " PC SP PS TEST# TCCM TCST"

EVEN  
ET2: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1  
000000

EM3: .ASCIZ "READY BIT DID NOT CAUSE AN INTERRUPT"

EH3: .ASCIZ " PC SP PS TEST# TCCM TCST"

EVEN  
ET3: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1  
000000

EM4: .ASCIZ "READY BIT CAUSED AN INTERRUPT WITH PROCESSOR AND TC11 AT SAME PRIORITY"

EH4: .ASCIZ " PC SP PS TEST# TCCM TCST"





3445	020006	020115	020040	052040	
3446	020014	051503	000124		
3447					.EVEN
3448	020020	001116	001176	001200	ET11: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
3449	020026	001174	001166	001164	
3450	020034	000000			000000
3451					
3452					
3453	020036	041524	052123	041040	EM12: .ASCIZ "TCST BIT 0 CAN BE SET WHILE IN MAINTNENCE MODE"
3454	020044	052111	030040	041440	
3455	020052	047101	041040	020105	
3456	020060	042523	020124	044127	
3457	020066	046111	020105	047111	
3458	020074	046440	044501	052116	
3459	020102	047101	047105	042503	
3460	020110	046440	042117	000105	
3461	020116	020040	041520	020040	EH12: .ASCIZ " PC SP PS TEST# TCCM TCST"
3462	020124	020040	020040	050123	
3463	020132	020040	020040	020040	
3464	020140	051520	020040	020040	
3465	020146	052040	051505	021524	
3466	020154	020040	052040	041503	
3467	020162	020115	020040	052040	
3468	020170	051503	000124		
3469					.EVEN
3470	020174	001116	001176	001200	ET12: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
3471	020202	001174	001166	001164	
3472	020210	000000			000000
3473					
3474					
3475	020212	041524	052123	041040	EM13: .ASCIZ "TCST BIT 1 CAN BE SET WHILE IN MAINTNENCE MODE"
3476	020220	052111	030040	041440	
3477	020226	047101	041040	020105	
3478	020234	042523	020124	044127	
3479	020242	046111	020105	047111	
3480	020250	046440	044501	052116	
3481	020256	047101	047105	042503	
3482	020264	046440	042117	000105	
3483	020272	020040	041520	020040	EH13: .ASCIZ " PC SP PS TEST# TCCM TCST"
3484	020300	020040	020040	050123	
3485	020306	020040	020040	020040	
3486	020314	051520	020040	020040	
3487	020322	052040	051505	021524	
3488	020330	020040	052040	041503	
3489	020336	020115	020040	052040	
3490	020344	051503	000124		
3491					.EVEN
3492	020350	001116	001176	001200	ET13: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
3493	020356	001174	001166	001164	
3494	020364	000000			000000
3495					
3496					
3497	020366	051127	046524	041440	EM14: .ASCIZ "WRTM COMMAND WITH WRTM SWITCH DISABLED FAILED TO SET ILO ERROR"
3498	020374	046517	040515	042116	
3499	020402	053440	052111	020110	
3500	020410	051127	046524	051440	



3501	020416	044527	041524	020110							
3502	020424	044504	040523	046102							
3503	020432	042105	043040	044501							
3504	020440	042514	020104	047524							
3505	020446	051440	052105	044440							
3506	020454	047514	042440	051122							
3507	020462	051117	000								
3508	020465	040	050040	020103	EH14:	.ASCIZ	" PC	SP	PS	TEST#	TCCM TCST"
3509	020472	020040	020040	051440							
3510	020500	020120	020040	020040							
3511	020506	051040	020123	020040							
3512	020514	020040	042524	052123							
3513	020522	020043	020040	041524							
3514	020530	046503	020040	020040							
3515	020536	041524	052123	000							
3516		020544			.EVEN						
3517	020544	001116	001176	001200	ET14:	\$ERRPC,	\$REG6,	\$REG7,	\$REG5,	\$REG2,	\$REG1
3518	020552	001174	001166	001164							
3519	020560	000000				000000					
3520											
3521											
3522	020562	046111	020117	051105	EM15:	.ASCIZ	"ILO ERROR FAILED TO SET THE 'ERROR' BIT"				
3523	020570	047522	020122	040506							
3524	020576	046111	042105	052040							
3525	020604	020117	042523	020124							
3526	020612	044124	020105	042447							
3527	020620	051122	051117	020047							
3528	020626	044502	000124								
3529	020632	020040	041520	020040	EH15:	.ASCIZ	" PC	SP	PS	TEST#	TCCM TCST"
3530	020640	020040	020040	050123							
3531	020646	020040	020040	020040							
3532	020654	051520	020040	020040							
3533	020662	052040	051505	021524							
3534	020670	020040	052040	041503							
3535	020676	020115	020040	052040							
3536	020704	051503	000124								
3537					.EVEN						
3538	020710	001116	001176	001200	ET15:	\$ERRPC,	\$REG6,	\$REG7,	\$REG5,	\$REG2,	\$REG1
3539	020716	001174	001166	001164							
3540	020724	000000				000000					
3541											
3542											
3543	020726	046103	040505	044522	EM16:	.ASCIZ	"CLEARING ILLEGAL OP FAILED TO CLEAR ILO ERROR"				
3544	020734	043516	044440	046114							
3545	020742	043505	046101	047440							
3546	020750	020120	040506	046111							
3547	020756	042105	052040	020117							
3548	020764	046103	040505	020122							
3549	020772	046111	020117	051105							
3550	021000	047522	000122								
3551	021004	020040	041520	020040	EH16:	.ASCIZ	" PC	SP	PS	TEST#	TCCM TCST"
3552	021012	020040	020040	050123							
3553	021020	020040	020040	020040							
3554	021026	051520	020040	020040							
3555	021034	052040	051505	021524							
3556	021042	020040	052040	041503							

3557	021050	020115	020040	052040	
3558	021056	051503	000124		
3559					EVEN
3560	021062	001116	001176	001200	ET16: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
3561	021070	001174	001166	001164	
3562	021076	000000			000000
3563					
3564					
3565	021100	046103	040505	044522	EM17: .ASCIZ "CLEARING ILLEGAL OP FAILED TO CLEAR THE 'ERROR' BIT"
3566	021106	043516	044440	046114	
3567	021114	043505	046101	047440	
3568	021122	020120	040506	046111	
3569	021130	042105	052040	020117	
3570	021136	046103	040505	020122	
3571	021144	044124	020105	042447	
3572	021152	051122	051117	020047	
3573	021160	044502	000124		
3574	021164	020040	041520	020040	EH17: .ASCIZ " PC SP PS TEST# TCCM TCST"
3575	021172	020040	020040	050123	
3576	021200	020040	020040	020040	
3577	021206	051520	020040	020040	
3578	021214	052040	051505	021524	
3579	021222	020040	052040	041503	
3580	021230	020115	020040	052040	
3581	021236	051503	000124		
3582					EVEN
3583	021242	001116	001176	001200	ET17: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
3584	021250	001174	001166	001164	
3585	021256	000000			000000
3586					
3587					
3588	021260	051127	046524	053440	EM20: .ASCIZ "WRTM WITH WRTM SWITCH OFF DID NOT SET ILO ERROR BIT"
3589	021266	052111	020110	051127	
3590	021274	046524	051440	044527	
3591	021302	041524	020110	043117	
3592	021310	020106	044504	020104	
3593	021316	047516	020124	042523	
3594	021324	020124	046111	020117	
3595	021332	051105	047522	020122	
3596	021340	044502	000124		
3597	021344	020040	041520	020040	EH20: .ASCIZ " PC SP PS TEST# TCCM TCST"
3598	021352	020040	020040	050123	
3599	021360	020040	020040	020040	
3600	021366	051520	020040	020040	
3601	021374	052040	051505	021524	
3602	021402	020040	052040	041503	
3603	021410	020115	020040	052040	
3604	021416	051503	000124		
3605					EVEN
3606	021422	001116	001176	001200	ET20: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
3607	021430	001174	001166	001164	
3608	021436	000000			000000
3609					
3610					
3611	021440	046111	020117	051105	EM21: .ASCIZ "ILO ERROR SETTING DID NOT CAUSE THE 'ERROR' BIT TO SET"
3612	021446	047522	020122	042523	

3613	021454	052124	047111	020107
3614	021462	044504	020104	047516
3615	021470	020124	040503	051525
3616	021476	020105	044124	020105
3617	021504	042447	051122	051117
3618	021512	020047	044502	020124
3619	021520	047524	051440	052105
3620	021526	000		
3621	021527	040	050040	020103
3622	021534	020040	020040	051440
3623	021540	020120	020040	020040
3624	021550	050040	020123	020040
3625	021556	020040	042524	052123
3626	021564	020043	020040	041524
3627	021572	046503	020040	020040
3628	021600	041524	052123	000
3629		021606		
3630	021606	001116	001176	001200
3631	021614	001174	001166	001164
3632	021622	000000		
3633				
3634				
3635	021624	046103	040505	044522
3636	021632	043516	042440	051122
3637	021640	051117	041040	052111
3638	021646	040440	051514	020117
3639	021654	046103	040505	042522
3640	021662	020104	046111	020117
3641	021670	051105	047522	000122
3642	021676	020040	041520	020040
3643	021704	020040	020040	050123
3644	021712	020040	020040	020040
3645	021720	051520	020040	020040
3646	021726	052040	051505	021524
3647	021734	020040	052040	041503
3648	021742	020115	020040	052040
3649	021750	051503	000124	
3650				
3651	021754	001116	001176	001200
3652	021762	001174	001166	001164
3653	021770	000000		
3654				
3655				
3656	021772	044124	020105	042447
3657	022000	051122	051117	020047
3658	022006	044502	020124	044504
3659	041014	020104	047516	020124
3660	041022	042523	000124	
3661	041030	041520	020040	020040
3662	041034	041040	020040	050123
3663	022042	020040	020040	020040
3664	022050	051520	020040	020040
3665	041056	052040	051505	021524
3666	041064	020040	052040	041503
3667	022072	020115	020040	052040
3668	022100	051503	000124	

EH21: .ASCIZ " PC SP PS TEST# TCCM TCST"

.EVEN  
ET21: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1  
000000

EM22: .ASCIZ "CLEARING ERROR BIT ALSO CLEARED ILO ERROR"

EH22: .ASCIZ " PC SP PS TEST# TCCM TCST"

.EVEN  
ET22: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1  
000000

EM23: .ASCIZ "THE 'ERROR' BIT DID NOT SET"

EH23: .ASCIZ " PC SP PS TEST# TCCM TCST"









3893	024176	027523	020102	040504						
3894	024204	040524	053440	051501						
3895	024212	000								
3896		024214			.EVEN					
3897	024214	001116	001176	001200	ET35:	SERRPC, SREG6, SREG7, SREG5, SREG2, SREG1, CRBUF, CRBUFA				
3898	024222	001174	001166	001164						
3899	024230	001270	001272							
3900	024234	040515	045522	052040	EM36:	.ASCIZ "MARK TRACK CODE 55 WAS MISTAKEN FOR END ZONE"				
3901	024242	040522	045503	041440						
3902	024250	042117	020105	032465						
3903	024256	053440	051501	046440						
3904	024264	051511	040524	042513						
3905	024272	020116	047506	020122						
3906	024300	047105	020104	047532						
3907	024306	042516	000							
3908	024311	040	050040	020103	EH36:	.ASCIZ " PC SP PS TEST# TCCM TCST"				
3909	024316	020040	020040	051440						
3910	024324	020120	020040	020040						
3911	024332	020040	020123	020040						
3912	024340	020040	042524	052123						
3913	024346	020043	020040	041524						
3914	024354	046503	020040	020040						
3915	024362	041524	052123	000						
3916		024370			.EVEN					
3917	024370	001116	001176	001200	ET36:	SERRPC, SREG6, SREG7, SREG5, SREG2, SREG1				
3918	024376	001174	001166	001164						
3919	024404	000000				000000				
3920										
3921										
3922	024406	051105	047522	000122	EM37:	.ASCIZ "ERROR"				
3923	024414	020040	041520	020040	EH37:	.ASCIZ " PC SP PS TEST# TCCM TCST"				
3924	024422	020040	020040	050123						
3925	024430	020040	020040	020040						
3926	024436	051520	020040	020040						
3927	024444	052040	051505	021524						
3928	024452	020040	052040	041503						
3929	024460	020115	020040	052040						
3930	024466	051503	000124							
3931					.EVEN					
3932	024472	001116	001176	001200	ET37:	SERRPC, SREG6, SREG7, SREG5, SREG2, SREG1				
3933	024500	001174	001166	001164						
3934	024506	000000				000000				
3935										
3936										
3937	024510	042522	042101	020131	EM40:	.ASCIZ "READY BIT DID NOT SET"				
3938	024516	044502	020124	044504						
3939	024524	020104	047516	020124						
3940	024532	042523	000124							
3941	024536	020040	041520	020040	EH40:	.ASCIZ " PC SP PS TEST# TCCM TCST"				
3942	024544	020040	020040	050123						
3943	024552	020040	020040	020040						
3944	024560	051520	020040	020040						
3945	024566	052040	051505	021524						
3946	024574	020040	052040	041503						
3947	024602	020115	020040	052040						
3948	024610	051503	000124							









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TC11 TEST #2  
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TRAP TABLE

4117	026260	051040	052502	025506	
4118	026266	000062			
4119					.EVEN
4120	026270	001116	001176	001200	ETS0: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1, RBUF+2
4121	026276	001174	001166	001164	
4122	026304	036310			
4123	026306	000000			000000
4124					
4125					
4126	026310	041524	040502	041440	EMS1: .ASCIZ "TCBA CONTAINS AN INCORRECT ADDRESS"
4127	026316	047117	040524	047111	
4128	026324	020123	047101	044440	
4129	026332	041516	051117	042522	
4130	026340	052103	040440	042104	
4131	026346	042522	051523	000	
4132	026353	040	050040	020103	EMS1: .ASCIZ " PC SP PS TEST# TCCM TCST TCBA TCBA S/B"
4133	026360	020040	020040	051440	
4134	026366	020120	020040	020040	
4135	026374	050040	020123	020040	
4136	026402	020040	042524	052123	
4137	026410	020043	020040	041524	
4138	026416	046503	020040	020040	
4139	026424	041524	052123	020040	
4140	026432	020040	041524	040502	
4141	026440	020040	052040	041103	
4142	026446	020101	027523	000102	
4143					.EVEN
4144	026454	001116	001176	001200	ETS1: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1, \$REG3, RBUF+512
4145	026462	001174	001166	001164	
4146	026470	001170	037020		
4147	026474	000000			000000
4148					
4149					
4150	026476	040520	051122	052111	EMS2: .ASCIZ "PARRITY ERROR WAS NOT DETECTED"
4151	026504	020131	051105	047522	
4152	026512	020122	040527	020123	
4153	026520	047516	020124	042504	
4154	026526	042524	052103	042105	
4155	026534	000			
4156	026535	040	050040	020103	EMS2: .ASCIZ " PC SP PS TEST# TCCM TCST TCWC"
4157	026542	020040	020040	051440	
4158	026550	020120	020040	020040	
4159	026556	050040	020123	020040	
4160	026564	020040	042524	052123	
4161	026572	020043	020040	041524	
4162	026600	046503	020040	020040	
4163	026606	041524	052123	020040	
4164	026614	020040	041524	041527	
4165	026622	000			
4166		026624			.EVEN
4167	026624	001116	001176	001200	ETS2: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1, \$REG0
4168	026632	001174	001166	001164	
4169	026640	001162			
4170	026642	000000			000000
4171					
4172					

4173	026644	040520	044522	054524
4174	026652	042440	051122	051117
4175	026660	042040	042111	047040
4176	026666	052117	051440	052105
4177	026674	052040	042510	023440
4178	026702	051105	047522	023522
4179	026710	041040	052111	000
4180	026715	040	050040	020103
4181	026722	020040	020040	051440
4182	026730	020120	020040	020040
4183	026736	050040	020123	020040
4184	026744	020040	042524	052123
4185	026752	020043	020040	041524
4186	026760	046503	020040	020040
4187	026766	041524	052123	020040
4188	026774	020040	041524	041527
4189	027002	000		
4190		027004		
4191	027004	001116	001176	001200
4192	027012	001174	001166	001164
4193	027020	001162		
4194	027022	000000		
4195				
4196				
4197	027024	040520	044522	054524
4198	027032	042440	051122	051117
4199	027040	041040	052111	053440
4200	027046	046111	020114	047516
4201	027054	020124	046103	040505
4202	027062	000122		
4203	027064	020040	041520	020040
4204	027072	020040	020040	050123
4205	027100	020040	020040	020040
4206	027106	051520	020040	020040
4207	027114	052040	051505	021524
4208	027122	020040	052040	041503
4209	027130	020115	020040	052040
4210	027136	051503	020124	020040
4211	027144	052040	053503	000103
4212				
4213	027152	001116	001176	001200
4214	027160	001174	001166	001164
4215	027166	001162		
4216	027170	000000		
4217				
4218				
4219	027172	046102	041517	020113
4220	027200	044515	051523	051440
4221	027206	047110	046125	020104
4222	027214	047516	020124	040510
4223	027222	042526	051440	052105
4224	027230	000		
4225	027231	040	050040	020103
4226	027236	020040	020040	051440
4227	027244	020120	020040	020040
4228	027252	050040	020123	020040

EM53: .ASCIZ "PARITY ERROR DID NOT SET THE 'ERROR' BIT"

EM53: .ASCIZ " PC SP PS TEST# TCCM TCST TCWC"

EVEN  
ETS3: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1, \$REG0

000000

EM54: .ASCIZ "PARITY ERROR BIT WILL NOT CLEAR"

EM54: .ASCIZ " PC SP PS TEST# TCCM TCST TCWC"

EVEN  
ETS4: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1, \$REG0

000000

EM55: .ASCIZ "BLOCK MISS SHOULD NOT HAVE SET"

EM55: .ASCIZ " PC SP PS TEST# TCCM TCST TCWC"

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TC11 TEST #2  
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TRAP TABLE

4229	027260	020040	042524	052123
4230	027256	041043	020040	041524
4231	027274	046503	040040	020040
4232	027302	041524	052123	020040
4233	027310	020040	041524	041527
4234	027316	000		
4235		027320		
4236	027320	001116	001176	001200
4237	027336	001174	001166	001164
4238	027334	001162		
4239	027336	000000		
4240				
4241				
4242	027340	042122	052101	020101
4243	027346	040527	020123	051511
4244	027354	051523	042105	041040
4245	027362	052125	041040	047514
4246	027370	045503	046440	051511
4247	027376	020123	040506	046111
4248	027404	042105	052040	020117
4249	027412	042523	000124	
4250	027416	021040	041520	020040
4251	027424	021040	020040	050123
4252	027432	020040	020040	020040
4253	027440	051520	020040	020040
4254	027446	052040	051505	021524
4255	027454	020040	052040	041503
4256	027462	020115	020040	052040
4257	027470	051503	020124	020040
4258	027476	052040	053503	000103
4259				
4260	027504	001116	001176	001200
4261	027512	001174	001166	001164
4262	027520	001162		
4263	027522	000000		
4264				
4265				
4266	027524	046102	041517	020113
4267	027532	044515	051523	051440
4268	027540	052105	044524	043516
4269	027546	042040	042111	047040
4270	027554	052117	051440	052105
4271	027562	052040	042510	023440
4272	027570	051105	047522	023522
4273	027576	041040	052111	000
4274	027603	040	050040	020103
4275	027610	020040	020040	051440
4276	027616	020120	020040	020040
4277	027624	050040	020123	020040
4278	027632	020040	042524	052123
4279	027640	020043	020040	041524
4280	027646	046503	020040	020040
4281	027654	041524	052123	020040
4282	027662	020040	041524	041527
4283	027670	000		
4284		027672		

.EVEN  
ETS5: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1, \$REG0

000000

EMS6: .ASCIZ "RDATA WAS ISSUED BUT BLOCK MISS FAILED TO SET"

EMS6: .ASCIZ " PC SP PS TEST# TCCM TCST TCWC"

.EVEN  
ETS6: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1, \$REG0

000000

EMS7: .ASCIZ "BLOCK MISS SETTING DID NOT SET THE 'ERROR' BIT"

EMS7: .ASCIZ " PC SP PS TEST# TCCM TCST TCWC"

.EVEN







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TRAP TABLE

4397	030726	051503	020124	020040	
4398	030734	052040	053503	000103	
4399					.EVEN
4400	030742	001116	001176	001200	ET64: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1, \$REG0
4401	030750	001174	001166	001164	
4402	030756	001162			
4403	030760	000000			000000
4404					
4405					
4406	030762	040504	040524	046440	EM65: .ASCIZ "DATA MISS SETTING DID NOT CAUSE THE 'ERROR' BIT TO SET"
4407	030770	051511	020123	042523	
4408	030776	052124	047111	020107	
4409	031004	044504	020104	047516	
4410	031012	020124	040503	051525	
4411	031020	020105	044124	020105	
4412	031026	042447	051122	051117	
4413	031034	020047	044502	020124	
4414	031042	051524	051440	052105	
4415	031050	000			
4416	031051	040	050040	020103	EM65: .ASCIZ " PC SP PS TEST# TCCM TCST"
4417	031056	020040	020040	051440	
4418	031064	020120	020040	020040	
4419	031072	050040	020123	020040	
4420	031100	020040	042524	052123	
4421	031106	020043	020040	041524	
4422	031114	046503	020040	020040	
4423	031122	041524	052123	000	
4424		031130			.EVEN
4425	031130	001116	001176	001200	ET65: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
4426	031136	001174	001166	001164	
4427	031144	000000			000000
4428					
4429					
4430	031146	046103	040505	044522	EM66: .ASCIZ "CLEARING THE 'ERROR' BIT DID NOT CAUSE DATA MISS TO BE CLEARED"
4431	031154	043516	052040	042510	
4432	031162	023440	051105	047522	
4433	031170	023527	041040	052111	
4434	031176	042040	042111	047040	
4435	031204	052117	041440	052501	
4436	031212	042523	042040	052101	
4437	031220	020101	044515	051523	
4438	031226	052040	020117	042502	
4439	031234	041440	042514	051101	
4440	031242	042105	000		
4441	031248	040	050040	020103	EM66: .ASCIZ " PC SP PS TEST# TCCM TCST"
4442	031252	020040	020040	051440	
4443	031260	020120	020040	020040	
4444	031266	050040	020123	020040	
4445	031274	020040	042524	052123	
4446	031302	020043	020040	041524	
4447	031310	046503	020040	020040	
4448	031316	041524	052123	000	
4449		031324			.EVEN
4450	031324	001116	001176	001200	ET66: \$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
4451	031332	001174	001166	001164	
4452	031340	000000			000000



Address	PC	SP	PS	TEST#	TCCM	TCST	TCWC
4509	031756	047111	020107	051127			
4510	031764	052111	020105	046101			
4511	031772	000114					
4512	031774	020040	041520	020040	EH71:	.ASCIZ	" PC SP PS TEST# TCCM TCST TCWC"
4513	032002	020040	020040	050123			
4514	032010	020040	020040	020040			
4515	032016	051520	020040	020040			
4516	032024	052040	051505	021524			
4517	032032	020040	052040	041503			
4518	032040	020115	020040	052040			
4519	032046	051503	020124	020040			
4520	032054	052040	053503	000103			
4521					.EVEN		
4522	032062	001116	001176	001200	ET71:	SERRPC, SREG6, SREG7, SREG5, SREG2, SREG1, TCWC	
4523	032070	001174	001166	001164			
4524	032076	001242					
4525	032100	000000				000000	
4526							
4527							
4528	032102	041524	040502	046440	EM72:	.ASCIZ	"TCBA MODIFIED DURING WRITE ALL"
4529	032110	042117	043111	042511			
4530	032116	020104	052504	051122			
4531	032124	047111	020107	051127			
4532	032132	052111	020105	046101			
4533	032140	000114					
4534	032142	020040	041520	020040	EH72:	.ASCIZ	" PC SP PS TEST# TCCM TCST TCBA"
4535	032150	020040	020040	050123			
4536	032156	020040	020040	020040			
4537	032164	051520	020040	020040			
4538	032172	052040	051505	021524			
4539	032200	020040	052040	041503			
4540	032206	020115	020040	052040			
4541	032214	051503	020124	020040			
4542	032222	052040	041103	000101			
4543					.EVEN		
4544	032230	001116	001176	001200	ET72:	SERRPC, SREG6, SREG7, SREG5, SREG2, SREG1, SREG3	
4545	032236	001174	001166	001164			
4546	032244	001170					
4547	032246	000000				000000	
4548							
4549							
4550	032250	051523	020124	044504	EM73:	.ASCIZ	"SST DID NOT CAUSE A SELECT ERROR"
4551	032256	020104	047516	020124			
4552	032264	040503	051525	020105			
4553	032272	020101	042523	042514			
4554	032280	052103	042440	051122			
4555	032306	051117	000				
4556	032311	040	050040	020103	EH73:	.ASCIZ	" PC SP PS TEST# TCCM TCST"
4557	032316	020040	020040	051440			
4558	032324	020120	020040	020040			
4559	032332	050040	020123	020040			
4560	032340	020040	042524	052123			
4561	032346	020043	020040	041524			
4562	032354	046503	020040	020040			
4563	032362	041524	052123	000			
4564	032370				.EVEN		

4565	032370	001116	001176	001200	ET73:	\$ERRPC, \$REG6, \$REG7, \$REG5, \$REG2, \$REG1
4566	032376	001174	001166	001164		
4567	032404	000000				000000
4568						
4569	032406	051124	050101	042520	EM74:	.ASCIZ "TRAPPED TO LOC 4 ATTEMPTING TO ACCESS TCCM"
4570	032414	020104	047524	046040		
4571	032422	041517	032040	040440		
4572	032430	052124	046505	052120		
4573	032436	047111	020107	047524		
4574	032444	040440	041503	051505		
4575	032452	020123	041524	046503		
4576	032460	000				
4577	032461	040	050040	020103	EH74:	.ASCIZ " PC SP PS TEST#"
4578	032466	020040	020040	051440		
4579	032474	020120	020040	020040		
4580	032502	050040	020123	020040		
4581	032510	020040	042524	052123		
4582	032516	000043				
4583					.EVEN	
4584	032520	001116	001176	001200	ET74:	\$ERRPC, \$REG6, \$REG7, \$REG5
4585	032526	001174				
4586	032530	000000				000000
4587	032532	051124	050101	042520	EM75:	.ASCIZ "TRAPPED TO LOC 4 ATTEMPTING TO ACCESS TCST"
4588	032540	020104	047524	046040		
4589	032546	041517	032040	040440		
4590	032554	052124	046505	052120		
4591	032562	047111	020107	047524		
4592	032570	040440	041503	051505		
4593	032576	020123	041524	052123		
4594	032604	000				
4595	032605	040	050040	020103	EH75:	.ASCIZ " PC SP PS TEST#"
4596	032612	020040	020040	051440		
4597	032620	020120	020040	020040		
4598	032626	050040	020123	020040		
4599	032634	020040	042524	052123		
4600	032642	000043				
4601					.EVEN	
4602	032644	001116	001176	001200	ET75:	\$ERRPC, \$REG6, \$REG7, \$REG5
4603	032652	001174				
4604	032654	000000				000000
4605	032656	051124	050101	042520	EM76:	.ASCIZ "TRAPPED TO LOC 4 ATTEMPTING TO ACCESS TCWC"
4606	032664	020104	047524	046040		
4607	032672	041517	032040	040440		
4608	032700	052124	046505	052120		
4609	032706	047111	020107	047524		
4610	032714	040440	041503	051505		
4611	032722	020123	041524	041527		
4612	032730	000				
4613	032731	040	050040	020103	EH76:	.ASCIZ " PC SP PS TEST#"
4614	032736	020040	020040	051440		
4615	032744	020120	020040	020040		
4616	032752	050040	020123	020040		
4617	032760	020040	042524	052123		
4618	032766	000043				
4619					.EVEN	
4620	032770	001116	001176	001200	ET76:	\$ERRPC, \$REG6, \$REG7, \$REG5

4621	032776	001174									
4622	033000	000000									
4623	033002	051124	050101	042520	EM77:	000000					
4624	033010	020104	047524	046040		.ASCIZ	"TRAPPED TO LOC 4 ATTEMPTING TO ACCESS TCBA"				
4625	033016	041517	032040	040440							
4626	033024	052124	046505	052120							
4627	033032	047111	020107	047524							
4628	033040	040440	041503	051505							
4629	033046	020123	041524	040502							
4630	033054	000									
4631	033055	040	050040	020103	EH77:	.ASCIZ	"	PC	SP	PS	TEST#"
4632	033062	020040	020040	051440							
4633	033070	020120	020040	020040							
4634	033076	050040	020123	020040							
4635	033104	020040	042524	052123							
4636	033112	000043									
4637											
4638	033114	001116	001176	001200	.EVEN						
4639	033122	001174			ET77:	SERRPC,	SREG6,	SREG7,	SREG5		
4640	033124	000000									
4641	033126				MTKC10:	000000					
4642	033126					C10	V7, V2, V7, V2, V7, V2				
4643	033126	034	010	074		.BYTE	0!V7, 0!V2, I!V7, 0!V2, 0!V7, 0!V2				; MTK CODE 10.
4644	033131	010	034	010							
4645	033134				MTKER:						
4646	033134					EMTE					
4647	033134	040	040	040		.BYTE	I, I, I, 0, 0, I				
4648	033137	000	000	040							
4649	033142				MTKEND:						
4650	033142					C22					
4651	033142	000	040	000		.BYTE	0, I, 0, 0, I, 0				; MTK CODE 22. FWD END ZONE.
4652	033145	000	040	000							
4653	033150				MTK55:						
4654	033150					C55					
4655	033150	040	000	040		.BYTE	I, 0, I, I, 0, I				; MTK CODE 55. REV END ZONE MARK.
4656	033153	040	000	040							
4657	033156				MTKSP:						
4658	033156					C10	V0, V6, V6, V6, V6, V6				
4659	033156	000	030	070		.BYTE	0!V0, 0!V6, I!V6, 0!V6, 0!V6, 0!V6				; MTK CODE 10.
4660	033161	030	030	030							
4661	033164				MTK7:						
4662	033164					C25					
4663	033164	000	040	000		.BYTE	0, I, 0, I, 0, I				; MTK CODE 25. EXTENSION MARK.
4664	033167	040	000	040							
4665	033172					C25					
4666	033172	000	040	000		.BYTE	0, I, 0, I, 0, I				; MTK CODE 25. EXTENSION MARK.
4667	033175	040	000	040							
4668	033200					C26	V0, V5, V2, V5, V2, V5				
4669	033200	000	064	010		.BYTE	0!V0, I!V5, 0!V2, I!V5, I!V2, 0!V5				; FWD BLOCK MARK.
4670	033203	064	050	024							
4671	033206					C32	V0, V5, V5, V5, V5, V5				
4672	033206	000	064	064		.BYTE	0!V0, I!V5, I!V5, 0!V5, I!V5, 0!V5				; REV GUARD.
4673	033211	024	064	024							
4674	033214				MTK5:						
4675	033214					C10	V0, V6, V6, V6, V6, V6				
4676	033214	000	030	070		.BYTE	0!V0, 0!V6, I!V6, 0!V6, 0!V6, 0!V6				; MTK CODE 10.

C08

INDEX-11-DZTCB-D TC11 TEST #2 MACY11 27(1006) 18-FEB-77 11:33 PAGE 86  
 DZTCB0.P11 18-FEB-77 10:59 TRAP TABLE

4677	033217	030	030	030			
4678	033222				MTK7A:		
4679	033222				C10	V0, V0, V0, V0, V0, V0	
4680	033222	000	000	040	.BYTE	0!V0, 0!V0, I!V0, 0!V0, 0!V0, 0!V0	; MTK CODE 10.
4681	033225	000	000	000			
4682	033230				MTK7B:		
4683	033230				C10	V0, V5, V0, V5, V0, V5	
4684	033230	000	024	040	.BYTE	0!V0, 0!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 10.
4685	033233	024	000	024			
4686	033236				MTKVAR:		
4687	033236				C10	V7, V2, V7, V2, V7, V2	
4688	033236	034	010	074	.BYTE	0!V7, 0!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 10.
4689	033241	010	034	010			
4690		000176			.REPT	126.	
4691					C70	V0, V5, V0, V5, V0, V5	
4692					C70	V7, V2, V7, V2, V7, V2	
4693					.ENOR		
4694	033244				C70	V0, V5, V0, V5, V0, V5	
4695	033244	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4696	033247	024	000	024			
4697	033252				C70	V7, V2, V7, V2, V7, V2	
4698	033252	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4699	033255	010	034	010			
4700	033260				C70	V0, V5, V0, V5, V0, V5	
4701	033260	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4702	033263	024	000	024			
4703	033266				C70	V7, V2, V7, V2, V7, V2	
4704	033266	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4705	033271	010	034	010			
4706	033274				C70	V0, V5, V0, V5, V0, V5	
4707	033274	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4708	033277	024	000	024			
4709	033302				C70	V7, V2, V7, V2, V7, V2	
4710	033302	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4711	033305	010	034	010			
4712	033310				C70	V0, V5, V0, V5, V0, V5	
4713	033310	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4714	033313	024	000	024			
4715	033316				C70	V7, V2, V7, V2, V7, V2	
4716	033316	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4717	033321	010	034	010			
4718	033324				C70	V0, V5, V0, V5, V0, V5	
4719	033324	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4720	033327	024	000	024			
4721	033332				C70	V7, V2, V7, V2, V7, V2	
4722	033332	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4723	033335	010	034	010			
4724	033340				C70	V0, V5, V0, V5, V0, V5	
4725	033340	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4726	033343	024	000	024			
4727	033346				C70	V7, V2, V7, V2, V7, V2	
4728	033346	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4729	033351	010	034	010			
4730	033354				C70	V0, V5, V0, V5, V0, V5	
4731	033354	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4732	033357	024	000	024			

4733	033362				C70	V7, V2, V7, V2, V7, V2	
4734	033363	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4735	033365	010	034	010			
4736	033370				C70	V0, V5, V0, V5, V0, V5	
4737	033370	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4738	033373	024	000	024			
4739	033376				C70	V7, V2, V7, V2, V7, V2	
4740	033376	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4741	033401	010	034	010			
4742	033404				C70	V0, V5, V0, V5, V0, V5	
4743	033404	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4744	033407	024	000	024			
4745	033412				C70	V7, V2, V7, V2, V7, V2	
4746	033412	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4747	033415	010	034	010			
4748	033420				C70	V0, V5, V0, V5, V0, V5	
4749	033420	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4750	033423	024	000	024			
4751	033426				C70	V7, V2, V7, V2, V7, V2	
4752	033426	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4753	033431	010	034	010			
4754	033434				C70	V0, V5, V0, V5, V0, V5	
4755	033434	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4756	033437	024	000	024			
4757	033442				C70	V7, V2, V7, V2, V7, V2	
4758	033442	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4759	033445	010	034	010			
4760	033450				C70	V0, V5, V0, V5, V0, V5	
4761	033450	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4762	033453	024	000	024			
4763	033456				C70	V7, V2, V7, V2, V7, V2	
4764	033456	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4765	033461	010	034	010			
4766	033464				C70	V0, V5, V0, V5, V0, V5	
4767	033464	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4768	033467	024	000	024			
4769	033472				C70	V7, V2, V7, V2, V7, V2	
4770	033472	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4771	033475	010	034	010			
4772	033500				C70	V0, V5, V0, V5, V0, V5	
4773	033500	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4774	033503	024	000	024			
4775	033506				C70	V7, V2, V7, V2, V7, V2	
4776	033506	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4777	033511	010	034	010			
4778	033514				C70	V0, V5, V0, V5, V0, V5	
4779	033514	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4780	033517	024	000	024			
4781	033522				C70	V7, V2, V7, V2, V7, V2	
4782	033522	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4783	033525	010	034	010			
4784	033530				C70	V0, V5, V0, V5, V0, V5	
4785	033530	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4786	033533	024	000	024			
4787	033536				C70	V7, V2, V7, V2, V7, V2	
4788	033536	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.

# E08

MAINDEC-11-DZTCB-D  
DZTCB0.P11

TC11 TEST #2  
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TRAP TABLE

4789	033541	010	034	010	C70	V0, V5, V0, V5, V0, V5	
4790	033544				.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4791	033544	040	064	040			
4792	033547	024	000	024			
4793	033552				C70	V7, V2, V7, V2, V7, V2	
4794	033552	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4795	033555	010	034	010			
4796	033560				C70	V0, V5, V0, V5, V0, V5	
4797	033560	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4798	033563	024	000	024			
4799	033566				C70	V7, V2, V7, V2, V7, V2	
4800	033566	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4801	033571	010	034	010			
4802	033574				C70	V0, V5, V0, V5, V0, V5	
4803	033574	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4804	033577	024	000	024			
4805	033602				C70	V7, V2, V7, V2, V7, V2	
4806	033602	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4807	033605	010	034	010			
4808	033610				C70	V0, V5, V0, V5, V0, V5	
4809	033610	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4810	033613	024	000	024			
4811	033616				C70	V7, V2, V7, V2, V7, V2	
4812	033616	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4813	033621	010	034	010			
4814	033624				C70	V0, V5, V0, V5, V0, V5	
4815	033624	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4816	033627	024	000	024			
4817	033632				C70	V7, V2, V7, V2, V7, V2	
4818	033632	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4819	033635	010	034	010			
4820	033640				C70	V0, V5, V0, V5, V0, V5	
4821	033640	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4822	033643	024	000	024			
4823	033646				C70	V7, V2, V7, V2, V7, V2	
4824	033646	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4825	033651	010	034	010			
4826	033654				C70	V0, V5, V0, V5, V0, V5	
4827	033654	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4828	033657	024	000	024			
4829	033662				C70	V7, V2, V7, V2, V7, V2	
4830	033662	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4831	033665	010	034	010			
4832	033670				C70	V0, V5, V0, V5, V0, V5	
4833	033670	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4834	033673	024	000	024			
4835	033676				C70	V7, V2, V7, V2, V7, V2	
4836	033676	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4837	033701	010	034	010			
4838	033704				C70	V0, V5, V0, V5, V0, V5	
4839	033704	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4840	033707	024	000	024			
4841	033712				C70	V7, V2, V7, V2, V7, V2	
4842	033712	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4843	033715	010	034	010			
4844	033720				C70	V0, V5, V0, V5, V0, V5	



# F08

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TC11 TEST #2  
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TRAP TABLE

4845	033720	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4846	033723	024	000	024			
4847	033726				C70	V7, V2, V7, V2, V7, V2	
4848	033726	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4849	033731	010	034	010			
4850	033734				C70	V0, V5, V0, V5, V0, V5	
4851	033734	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4852	033737	024	000	024			
4853	033742				C70	V7, V2, V7, V2, V7, V2	
4854	033742	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4855	033745	010	034	010			
4856	033750				C70	V0, V5, V0, V5, V0, V5	
4857	033750	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4858	033753	024	000	024			
4859	033756				C70	V7, V2, V7, V2, V7, V2	
4860	033756	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4861	033761	010	034	010			
4862	033764				C70	V0, V5, V0, V5, V0, V5	
4863	033764	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4864	033767	024	000	024			
4865	033772				C70	V7, V2, V7, V2, V7, V2	
4866	033772	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4867	033775	010	034	010			
4868	034000				C70	V0, V5, V0, V5, V0, V5	
4869	034000	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4870	034003	024	000	024			
4871	034006				C70	V7, V2, V7, V2, V7, V2	
4872	034006	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4873	034011	010	034	010			
4874	034014				C70	V0, V5, V0, V5, V0, V5	
4875	034014	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4876	034017	024	000	024			
4877	034022				C70	V7, V2, V7, V2, V7, V2	
4878	034022	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4879	034025	010	034	010			
4880	034030				C70	V0, V5, V0, V5, V0, V5	
4881	034030	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4882	034033	024	000	024			
4883	034036				C70	V7, V2, V7, V2, V7, V2	
4884	034036	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4885	034041	010	034	010			
4886	034044				C70	V0, V5, V0, V5, V0, V5	
4887	034044	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4888	034047	024	000	024			
4889	034052				C70	V7, V2, V7, V2, V7, V2	
4890	034052	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4891	034055	010	034	010			
4892	034060				C70	V0, V5, V0, V5, V0, V5	
4893	034060	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4894	034063	024	000	024			
4895	034066				C70	V7, V2, V7, V2, V7, V2	
4896	034066	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4897	034071	010	034	010			
4898	034074				C70	V0, V5, V0, V5, V0, V5	
4899	034074	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4900	034077	024	000	024			

4901	074	050	074
4902	010	034	010
4903			
4904			
4905	040	064	040
4906	024	000	024
4907			
4908	072	050	074
4909	010	034	010
4910			
4911	030	064	040
4912	024	000	024
4913			
4914	074	050	074
4915	010	034	010
4916			
4917	040	064	040
4918	024	000	024
4919			
4920	074	050	074
4921	010	034	010
4922			
4923	030	064	040
4924	024	000	024
4925			
4926	074	050	074
4927	010	034	010
4928			
4929	040	064	040
4930	024	000	024
4931			
4932	074	050	074
4933	010	034	010
4934			
4935	040	064	040
4936	024	000	024
4937			
4938	074	050	074
4939	010	034	010
4940			
4941	040	064	040
4942	024	000	024
4943			
4944	074	050	074
4945	010	034	010
4946			
4947	040	064	040
4948	024	000	024
4949			
4950	074	050	074
4951	010	034	010
4952			
4953	040	064	040
4954	024	000	024
4955			
4956	074	050	074

C70	V7, V2, V7, V2, V7, V2	
.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
C70	V0, V5, V0, V5, V0, V5	
.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
C70	V7, V2, V7, V2, V7, V2	
.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
C70	V0, V5, V0, V5, V0, V5	
.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
C70	V7, V2, V7, V2, V7, V2	
.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
C70	V0, V5, V0, V5, V0, V5	
.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
C70	V7, V2, V7, V2, V7, V2	
.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
C70	V0, V5, V0, V5, V0, V5	
.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
C70	V7, V2, V7, V2, V7, V2	
.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
C70	V0, V5, V0, V5, V0, V5	
.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
C70	V7, V2, V7, V2, V7, V2	
.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
C70	V0, V5, V0, V5, V0, V5	
.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
C70	V7, V2, V7, V2, V7, V2	
.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
C70	V0, V5, V0, V5, V0, V5	
.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
C70	V7, V2, V7, V2, V7, V2	
.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.

# H08

MAINDEC-11-DZTCB-D TC11 TEST #2  
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 TRAP TABLE

4957	034261	010	034	010	C70	V0, V5, V0, V5, V0, V5	
4958	034264				.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4959	034264	040	064	040			
4960	034267	024	000	024			
4961	034272				C70	V7, V2, V7, V2, V7, V2	
4962	034272	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4963	034275	010	034	010			
4964	034300				C70	V0, V5, V0, V5, V0, V5	
4965	034300	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4966	034303	024	000	024			
4967	034306				C70	V7, V2, V7, V2, V7, V2	
4968	034306	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4969	034311	010	034	010			
4970	034314				C70	V0, V5, V0, V5, V0, V5	
4971	034314	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4972	034317	024	000	024			
4973	034322				C70	V7, V2, V7, V2, V7, V2	
4974	034322	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4975	034325	010	034	010			
4976	034330				C70	V0, V5, V0, V5, V0, V5	
4977	034330	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4978	034333	024	000	024			
4979	034336				C70	V7, V2, V7, V2, V7, V2	
4980	034336	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4981	034341	010	034	010			
4982	034344				C70	V0, V5, V0, V5, V0, V5	
4983	034344	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4984	034347	024	000	024			
4985	034352				C70	V7, V2, V7, V2, V7, V2	
4986	034352	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4987	034355	010	034	010			
4988	034360				C70	V0, V5, V0, V5, V0, V5	
4989	034360	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4990	034363	024	000	024			
4991	034366				C70	V7, V2, V7, V2, V7, V2	
4992	034366	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4993	034371	010	034	010			
4994	034374				C70	V0, V5, V0, V5, V0, V5	
4995	034374	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
4996	034377	024	000	024			
4997	034402				C70	V7, V2, V7, V2, V7, V2	
4998	034402	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
4999	034405	010	034	010			
5000	034410				C70	V0, V5, V0, V5, V0, V5	
5001	034410	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5002	034413	024	000	024			
5003	034416				C70	V7, V2, V7, V2, V7, V2	
5004	034416	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5005	034421	010	034	010			
5006	034424				C70	V0, V5, V0, V5, V0, V5	
5007	034424	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5008	034427	024	000	024			
5009	034430				C70	V7, V2, V7, V2, V7, V2	
5010	034430	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5011	034435	010	034	010			
5012	034440				C70	V0, V5, V0, V5, V0, V5	

5013	034440	040	064	040	.BYTE	I!V0,I!V5,I!V0,O!V5,O!V0,O!V5	;MTK CODE 70. DATA MARK.
5014	034443	024	000	024			
5015	034446				C70	V7,V2,V7,V2,V7,V2	
5016	034446	074	050	074	.BYTE	I!V7,I!V2,I!V7,O!V2,O!V7,O!V2	;MTK CODE 70. DATA MARK.
5017	034451	010	034	010			
5018	034454				C70	V0,V5,V0,V5,V0,V5	
5019	034454	040	064	040	.BYTE	I!V0,I!V5,I!V0,O!V5,O!V0,O!V5	;MTK CODE 70. DATA MARK.
5020	034457	024	000	024			
5021	034462				C70	V7,V2,V7,V2,V7,V2	
5022	034462	074	050	074	.BYTE	I!V7,I!V2,I!V7,O!V2,O!V7,O!V2	;MTK CODE 70. DATA MARK.
5023	034465	010	034	010			
5024	034470				C70	V0,V5,V0,V5,V0,V5	
5025	034470	040	064	040	.BYTE	I!V0,I!V5,I!V0,O!V5,O!V0,O!V5	;MTK CODE 70. DATA MARK.
5026	034473	024	000	024			
5027	034476				C70	V7,V2,V7,V2,V7,V2	
5028	034476	074	050	074	.BYTE	I!V7,I!V2,I!V7,O!V2,O!V7,O!V2	;MTK CODE 70. DATA MARK.
5029	034501	010	034	010			
5030	034504				C70	V0,V5,V0,V5,V0,V5	
5031	034504	040	064	040	.BYTE	I!V0,I!V5,I!V0,O!V5,O!V0,O!V5	;MTK CODE 70. DATA MARK.
5032	034507	024	000	024			
5033	034512				C70	V7,V2,V7,V2,V7,V2	
5034	034512	074	050	074	.BYTE	I!V7,I!V2,I!V7,O!V2,O!V7,O!V2	;MTK CODE 70. DATA MARK.
5035	034515	010	034	010			
5036	034520				C70	V0,V5,V0,V5,V0,V5	
5037	034520	040	064	040	.BYTE	I!V0,I!V5,I!V0,O!V5,O!V0,O!V5	;MTK CODE 70. DATA MARK.
5038	034523	024	000	024			
5039	034526				C70	V7,V2,V7,V2,V7,V2	
5040	034526	074	050	074	.BYTE	I!V7,I!V2,I!V7,O!V2,O!V7,O!V2	;MTK CODE 70. DATA MARK.
5041	034531	010	034	010			
5042	034534				C70	V0,V5,V0,V5,V0,V5	
5043	034534	040	064	040	.BYTE	I!V0,I!V5,I!V0,O!V5,O!V0,O!V5	;MTK CODE 70. DATA MARK.
5044	034537	024	000	024			
5045	034542				C70	V7,V2,V7,V2,V7,V2	
5046	034542	074	050	074	.BYTE	I!V7,I!V2,I!V7,O!V2,O!V7,O!V2	;MTK CODE 70. DATA MARK.
5047	034545	010	034	010			
5048	034550				C70	V0,V5,V0,V5,V0,V5	
5049	034550	040	064	040	.BYTE	I!V0,I!V5,I!V0,O!V5,O!V0,O!V5	;MTK CODE 70. DATA MARK.
5050	034553	024	000	024			
5051	034556				C70	V7,V2,V7,V2,V7,V2	
5052	034556	074	050	074	.BYTE	I!V7,I!V2,I!V7,O!V2,O!V7,O!V2	;MTK CODE 70. DATA MARK.
5053	034561	010	034	010			
5054	034564				C70	V0,V5,V0,V5,V0,V5	
5055	034564	040	064	040	.BYTE	I!V0,I!V5,I!V0,O!V5,O!V0,O!V5	;MTK CODE 70. DATA MARK.
5056	034567	024	000	024			
5057	034572				C70	V7,V2,V7,V2,V7,V2	
5058	034572	074	050	074	.BYTE	I!V7,I!V2,I!V7,O!V2,O!V7,O!V2	;MTK CODE 70. DATA MARK.
5059	034575	010	034	010			
5060	034600				C70	V0,V5,V0,V5,V0,V5	
5061	034600	040	064	040	.BYTE	I!V0,I!V5,I!V0,O!V5,O!V0,O!V5	;MTK CODE 70. DATA MARK.
5062	034603	024	000	024			
5063	034606				C70	V7,V2,V7,V2,V7,V2	
5064	034606	074	050	074	.BYTE	I!V7,I!V2,I!V7,O!V2,O!V7,O!V2	;MTK CODE 70. DATA MARK.
5065	034611	010	034	010			
5066	034614				C70	V0,V5,V0,V5,V0,V5	
5067	034614	040	064	040	.BYTE	I!V0,I!V5,I!V0,O!V5,O!V0,O!V5	;MTK CODE 70. DATA MARK.
5068	034617	024	000	024			

# JOB

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DZTCB0.P11

TC11 TEST #2  
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TRAP TABLE

5069	034622				C70	V7, V2, V7, V2, V7, V2	
5070	034622	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5071	034623	010	034	010			
5072	034630				C70	V0, V5, V0, V5, V0, V5	
5073	034630	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5074	034633	024	000	024			
5075	034636				C70	V7, V2, V7, V2, V7, V2	
5076	034636	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5077	034641	010	034	010			
5078	034644				C70	V0, V5, V0, V5, V0, V5	
5079	034644	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5080	034647	024	000	024			
5081	034652				C70	V7, V2, V7, V2, V7, V2	
5082	034652	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5083	034655	010	034	010			
5084	034650				C70	V0, V5, V0, V5, V0, V5	
5085	034650	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5086	034653	024	000	024			
5087	034666				C70	V7, V2, V7, V2, V7, V2	
5088	034666	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5089	034671	010	034	010			
5090	034674				C70	V0, V5, V0, V5, V0, V5	
5091	034674	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5092	034677	024	000	024			
5093	034702				C70	V7, V2, V7, V2, V7, V2	
5094	034702	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5095	034705	010	034	010			
5096	034710				C70	V0, V5, V0, V5, V0, V5	
5097	034710	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5098	034713	024	000	024			
5099	034716				C70	V7, V2, V7, V2, V7, V2	
5100	034716	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5101	034721	010	034	010			
5102	034724				C70	V0, V5, V0, V5, V0, V5	
5103	034724	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5104	034727	024	000	024			
5105	034732				C70	V7, V2, V7, V2, V7, V2	
5106	034732	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5107	034735	010	034	010			
5108	034740				C70	V0, V5, V0, V5, V0, V5	
5109	034740	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5110	034743	024	000	024			
5111	034746				C70	V7, V2, V7, V2, V7, V2	
5112	034746	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5113	034751	010	034	010			
5114	034754				C70	V0, V5, V0, V5, V0, V5	
5115	034754	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5116	034757	024	000	024			
5117	034762				C70	V7, V2, V7, V2, V7, V2	
5118	034762	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5119	034765	010	034	010			
5120	034770				C70	V0, V5, V0, V5, V0, V5	
5121	034770	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5122	034773	024	000	024			
5123	034776				C70	V7, V2, V7, V2, V7, V2	
5124	034776	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.

# K08

MAINDEC-11-DZTCB-D  
DZTCB0.P11

TC11 TEST #2  
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TRAP TABLE

5125	035001	010	034	010		
5126	035004				C70	V0, V5, V0, V5, V0, V5
5127	035004	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5 ; MTK CODE 70. DATA MARK.
5128	035007	024	000	024		
5129	035012				C70	V7, V2, V7, V2, V7, V2
5130	035012	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2 ; MTK CODE 70. DATA MARK.
5131	035015	010	034	010		
5132	035020				C70	V0, V5, V0, V5, V0, V5
5133	035020	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5 ; MTK CODE 70. DATA MARK.
5134	035023	024	000	024		
5135	035026				C70	V7, V2, V7, V2, V7, V2
5136	035026	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2 ; MTK CODE 70. DATA MARK.
5137	035031	010	034	010		
5138	035034				C70	V0, V5, V0, V5, V0, V5
5139	035034	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5 ; MTK CODE 70. DATA MARK.
5140	035037	024	000	024		
5141	035042				C70	V7, V2, V7, V2, V7, V2
5142	035042	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2 ; MTK CODE 70. DATA MARK.
5143	035045	010	034	010		
5144	035050				C70	V0, V5, V0, V5, V0, V5
5145	035050	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5 ; MTK CODE 70. DATA MARK.
5146	035053	024	000	024		
5147	035056				C70	V7, V2, V7, V2, V7, V2
5148	035056	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2 ; MTK CODE 70. DATA MARK.
5149	035061	010	034	010		
5150	035064				C70	V0, V5, V0, V5, V0, V5
5151	035064	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5 ; MTK CODE 70. DATA MARK.
5152	035067	024	000	024		
5153	035072				C70	V7, V2, V7, V2, V7, V2
5154	035072	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2 ; MTK CODE 70. DATA MARK.
5155	035075	010	034	010		
5156	035100				C70	V0, V5, V0, V5, V0, V5
5157	035100	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5 ; MTK CODE 70. DATA MARK.
5158	035103	024	000	024		
5159	035106				C70	V7, V2, V7, V2, V7, V2
5160	035106	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2 ; MTK CODE 70. DATA MARK.
5161	035111	010	034	010		
5162	035114				C70	V0, V5, V0, V5, V0, V5
5163	035114	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5 ; MTK CODE 70. DATA MARK.
5164	035117	024	000	024		
5165	035123				C70	V7, V2, V7, V2, V7, V2
5166	035123	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2 ; MTK CODE 70. DATA MARK.
5167	035125	010	034	010		
5168	035130				C70	V0, V5, V0, V5, V0, V5
5169	035130	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5 ; MTK CODE 70. DATA MARK.
5170	035133	024	000	024		
5171	035136				C70	V7, V2, V7, V2, V7, V2
5172	035136	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2 ; MTK CODE 70. DATA MARK.
5173	035141	010	034	010		
5174	035144				C70	V0, V5, V0, V5, V0, V5
5175	035144	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5 ; MTK CODE 70. DATA MARK.
5176	035147	024	000	024		
5177	035152				C70	V7, V2, V7, V2, V7, V2
5178	035152	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2 ; MTK CODE 70. DATA MARK.
5179	035155	010	034	010		
5180	035160				C70	V0, V5, V0, V5, V0, V5

5181	035160	040	064	040	.BYTE	I!V0,I!V5,I!V0,0!V5,0!V0,0!V5	;MTK CODE 70. DATA MARK.
5182	035163	024	000	024			
5183	035166				C70	V7,V2,V7,V2,V7,V2	
5184	035166	074	050	074	.BYTE	I!V7,I!V2,I!V7,0!V2,0!V7,0!V2	;MTK CODE 70. DATA MARK.
5185	035171	010	034	010			
5186	035174				C70	V0,V5,V0,V5,V0,V5	
5187	035174	040	064	040	.BYTE	I!V0,I!V5,I!V0,0!V5,0!V0,0!V5	;MTK CODE 70. DATA MARK.
5188	035177	024	000	024			
5189	035209				C70	V7,V2,V7,V2,V7,V2	
5190	035209	074	050	074	.BYTE	I!V7,I!V2,I!V7,0!V2,0!V7,0!V2	;MTK CODE 70. DATA MARK.
5191	035205	010	034	010			
5192	035210				C70	V0,V5,V0,V5,V0,V5	
5193	035210	040	064	040	.BYTE	I!V0,I!V5,I!V0,0!V5,0!V0,0!V5	;MTK CODE 70. DATA MARK.
5194	035213	024	000	024			
5195	035216				C70	V7,V2,V7,V2,V7,V2	
5196	035216	074	050	074	.BYTE	I!V7,I!V2,I!V7,0!V2,0!V7,0!V2	;MTK CODE 70. DATA MARK.
5197	035221	010	034	010			
5198	035224				C70	V0,V5,V0,V5,V0,V5	
5199	035224	040	064	040	.BYTE	I!V0,I!V5,I!V0,0!V5,0!V0,0!V5	;MTK CODE 70. DATA MARK.
5200	035227	024	000	024			
5201	035232				C70	V7,V2,V7,V2,V7,V2	
5202	035232	074	050	074	.BYTE	I!V7,I!V2,I!V7,0!V2,0!V7,0!V2	;MTK CODE 70. DATA MARK.
5203	035235	010	034	010			
5204	035240				C70	V0,V5,V0,V5,V0,V5	
5205	035240	040	064	040	.BYTE	I!V0,I!V5,I!V0,0!V5,0!V0,0!V5	;MTK CODE 70. DATA MARK.
5206	035243	024	000	024			
5207	035246				C70	V7,V2,V7,V2,V7,V2	
5208	035246	074	050	074	.BYTE	I!V7,I!V2,I!V7,0!V2,0!V7,0!V2	;MTK CODE 70. DATA MARK.
5209	035251	010	034	010			
5210	035254				C70	V0,V5,V0,V5,V0,V5	
5211	035254	040	064	040	.BYTE	I!V0,I!V5,I!V0,0!V5,0!V0,0!V5	;MTK CODE 70. DATA MARK.
5212	035257	024	000	024			
5213	035262				C70	V7,V2,V7,V2,V7,V2	
5214	035262	074	050	074	.BYTE	I!V7,I!V2,I!V7,0!V2,0!V7,0!V2	;MTK CODE 70. DATA MARK.
5215	035265	010	034	010			
5216	035270				C70	V0,V5,V0,V5,V0,V5	
5217	035270	040	064	040	.BYTE	I!V0,I!V5,I!V0,0!V5,0!V0,0!V5	;MTK CODE 70. DATA MARK.
5218	035273	024	000	024			
5219	035276				C70	V7,V2,V7,V2,V7,V2	
5220	035276	074	050	074	.BYTE	I!V7,I!V2,I!V7,0!V2,0!V7,0!V2	;MTK CODE 70. DATA MARK.
5221	035301	010	034	010			
5222	035304				C70	V0,V5,V0,V5,V0,V5	
5223	035304	040	064	040	.BYTE	I!V0,I!V5,I!V0,0!V5,0!V0,0!V5	;MTK CODE 70. DATA MARK.
5224	035307	024	000	024			
5225	035312				C70	V7,V2,V7,V2,V7,V2	
5226	035312	074	050	074	.BYTE	I!V7,I!V2,I!V7,0!V2,0!V7,0!V2	;MTK CODE 70. DATA MARK.
5227	035315	010	034	010			
5228	035320				C70	V0,V5,V0,V5,V0,V5	
5229	035320	040	064	040	.BYTE	I!V0,I!V5,I!V0,0!V5,0!V0,0!V5	;MTK CODE 70. DATA MARK.
5230	035323	024	000	024			
5231	035326				C70	V7,V2,V7,V2,V7,V2	
5232	035326	074	050	074	.BYTE	I!V7,I!V2,I!V7,0!V2,0!V7,0!V2	;MTK CODE 70. DATA MARK.
5233	035331	010	034	010			
5234	035334				C70	V0,V5,V0,V5,V0,V5	
5235	035334	040	064	040	.BYTE	I!V0,I!V5,I!V0,0!V5,0!V0,0!V5	;MTK CODE 70. DATA MARK.
5236	035337	024	000	024			

M08

MRINDEC-11-DZTCB-D TC11 TEST #2  
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 TRAP TABLE

5237	035342	074	050	074	C70	V7, V2, V7, V2, V7, V2	
5238	035342	010	034	010	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5239	035345						
5240	035350	040	064	040	C70	V0, V5, V0, V5, V0, V5	
5241	035350	024	000	024	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5242	035353						
5243	035356	074	050	074	C70	V7, V2, V7, V2, V7, V2	
5244	035356	010	034	010	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5245	035361						
5246	035364	040	064	040	C70	V0, V5, V0, V5, V0, V5	
5247	035364	024	000	024	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5248	035367						
5249	035372	074	050	074	C70	V7, V2, V7, V2, V7, V2	
5250	035372	010	034	010	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5251	035375						
5252	035400	040	064	040	C70	V0, V5, V0, V5, V0, V5	
5253	035400	024	000	024	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5254	035403						
5255	035406	074	050	074	C70	V7, V2, V7, V2, V7, V2	
5256	035406	010	034	010	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5257	035411						
5258	035414	040	064	040	C70	V0, V5, V0, V5, V0, V5	
5259	035414	024	000	024	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5260	035417						
5261	035422	074	050	074	C70	V7, V2, V7, V2, V7, V2	
5262	035422	010	034	010	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5263	035425						
5264	035430	040	064	040	C70	V0, V5, V0, V5, V0, V5	
5265	035430	024	000	024	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5266	035433						
5267	035436	074	050	074	C70	V7, V2, V7, V2, V7, V2	
5268	035436	010	034	010	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5269	035441						
5270	035444	040	064	040	C70	V0, V5, V0, V5, V0, V5	
5271	035444	024	000	024	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5272	035447						
5273	035452	074	050	074	C70	V7, V2, V7, V2, V7, V2	
5274	035452	010	034	010	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5275	035455						
5276	035460	040	064	040	C70	V0, V5, V0, V5, V0, V5	
5277	035460	024	000	024	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5278	035463						
5279	035466	074	050	074	C70	V7, V2, V7, V2, V7, V2	
5280	035466	010	034	010	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5281	035471						
5282	035474	040	064	040	C70	V0, V5, V0, V5, V0, V5	
5283	035474	024	000	024	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5284	035477						
5285	035502	074	050	074	C70	V7, V2, V7, V2, V7, V2	
5286	035502	010	034	010	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5287	035505						
5288	035510	040	064	040	C70	V0, V5, V0, V5, V0, V5	
5289	035510	024	000	024	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5290	035513						
5291	035516	074	050	074	C70	V7, V2, V7, V2, V7, V2	
5292	035516				.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.



# N08

MAINDEC-11-DZTCB-D TC11 TEST #2 MACY11 27(1006) 18-FEB-77 11:33 PAGE 97  
 DZTCB0.P11 18-FEB-77 10:59 TRAP TABLE

5293	035521	010	034	010		
5294	035524				C70	V0, V5, V0, V5, V0, V5
5295	035524	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5 ; MTK CODE 70. DATA MARK.
5296	035527	024	000	024		
5297	035532				C70	V7, V2, V7, V2, V7, V2
5298	035532	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2 ; MTK CODE 70. DATA MARK.
5299	035535	010	034	010		
5300	035540				C70	V0, V5, V0, V5, V0, V5
5301	035540	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5 ; MTK CODE 70. DATA MARK.
5302	035543	024	000	024		
5303	035546				C70	V7, V2, V7, V2, V7, V2
5304	035546	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2 ; MTK CODE 70. DATA MARK.
5305	035551	010	034	010		
5306	035554				C70	V0, V5, V0, V5, V0, V5
5307	035554	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5 ; MTK CODE 70. DATA MARK.
5308	035557	024	000	024		
5309	035562				C70	V7, V2, V7, V2, V7, V2
5310	035562	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2 ; MTK CODE 70. DATA MARK.
5311	035565	010	034	010		
5312	035570				C70	V0, V5, V0, V5, V0, V5
5313	035570	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5 ; MTK CODE 70. DATA MARK.
5314	035573	024	000	024		
5315	035576				C70	V7, V2, V7, V2, V7, V2
5316	035576	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2 ; MTK CODE 70. DATA MARK.
5317	035601	010	034	010		
5318	035604				C70	V0, V5, V0, V5, V0, V5
5319	035604	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5 ; MTK CODE 70. DATA MARK.
5320	035607	024	000	024		
5321	035612				C70	V7, V2, V7, V2, V7, V2
5322	035612	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2 ; MTK CODE 70. DATA MARK.
5323	035615	010	034	010		
5324	035620				C70	V0, V5, V0, V5, V0, V5
5325	035620	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5 ; MTK CODE 70. DATA MARK.
5326	035623	024	000	024		
5327	035626				C70	V7, V2, V7, V2, V7, V2
5328	035626	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2 ; MTK CODE 70. DATA MARK.
5329	035631	010	034	010		
5330	035634				C70	V0, V5, V0, V5, V0, V5
5331	035634	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5 ; MTK CODE 70. DATA MARK.
5332	035637	024	000	024		
5333	035642				C70	V7, V2, V7, V2, V7, V2
5334	035642	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2 ; MTK CODE 70. DATA MARK.
5335	035645	010	034	010		
5336	035650				C70	V0, V5, V0, V5, V0, V5
5337	035650	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5 ; MTK CODE 70. DATA MARK.
5338	035653	024	000	024		
5339	035656				C70	V7, V2, V7, V2, V7, V2
5340	035656	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2 ; MTK CODE 70. DATA MARK.
5341	035661	010	034	010		
5342	035664				C70	V0, V5, V0, V5, V0, V5
5343	035664	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5 ; MTK CODE 70. DATA MARK.
5344	035667	024	000	024		
5345	035672				C70	V7, V2, V7, V2, V7, V2
5346	035672	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2 ; MTK CODE 70. DATA MARK.
5347	035675	010	034	010		
5348	035700				C70	V0, V5, V0, V5, V0, V5

5349	035700	040	064	040	.BYTE	I!V0,I!V5,I!V0,0!V5,0!V0,0!V5	;MTK CODE 70. DATA MARK.
5350	035703	024	000	024			
5351	035706				C70	V7,V2,V7,V2,V7,V2	
5352	035706	074	050	074	.BYTE	I!V7,I!V2,I!V7,0!V2,0!V7,0!V2	;MTK CODE 70. DATA MARK.
5353	035711	010	034	010			
5354	035714				C70	V0,V5,V0,V5,V0,V5	
5355	035714	040	064	040	.BYTE	I!V0,I!V5,I!V0,0!V5,0!V0,0!V5	;MTK CODE 70. DATA MARK.
5356	035717	024	000	024			
5357	035722				C70	V7,V2,V7,V2,V7,V2	
5358	035722	074	050	074	.BYTE	I!V7,I!V2,I!V7,0!V2,0!V7,0!V2	;MTK CODE 70. DATA MARK.
5359	035725	010	034	010			
5360	035730				C70	V0,V5,V0,V5,V0,V5	
5361	035730	040	064	040	.BYTE	I!V0,I!V5,I!V0,0!V5,0!V0,0!V5	;MTK CODE 70. DATA MARK.
5362	035733	024	000	024			
5363	035736				C70	V7,V2,V7,V2,V7,V2	
5364	035736	074	050	074	.BYTE	I!V7,I!V2,I!V7,0!V2,0!V7,0!V2	;MTK CODE 70. DATA MARK.
5365	035741	010	034	010			
5366	035744				C70	V0,V5,V0,V5,V0,V5	
5367	035744	040	064	040	.BYTE	I!V0,I!V5,I!V0,0!V5,0!V0,0!V5	;MTK CODE 70. DATA MARK.
5368	035747	024	000	024			
5369	035752				C70	V7,V2,V7,V2,V7,V2	
5370	035752	074	050	074	.BYTE	I!V7,I!V2,I!V7,0!V2,0!V7,0!V2	;MTK CODE 70. DATA MARK.
5371	035755	010	034	010			
5372	035760				C70	V0,V5,V0,V5,V0,V5	
5373	035760	040	064	040	.BYTE	I!V0,I!V5,I!V0,0!V5,0!V0,0!V5	;MTK CODE 70. DATA MARK.
5374	035763	024	000	024			
5375	035766				C70	V7,V2,V7,V2,V7,V2	
5376	035766	074	050	074	.BYTE	I!V7,I!V2,I!V7,0!V2,0!V7,0!V2	;MTK CODE 70. DATA MARK.
5377	035771	010	034	010			
5378	035774				C70	V0,V5,V0,V5,V0,V5	
5379	035774	040	064	040	.BYTE	I!V0,I!V5,I!V0,0!V5,0!V0,0!V5	;MTK CODE 70. DATA MARK.
5380	035777	024	000	024			
5381	036002				C70	V7,V2,V7,V2,V7,V2	
5382	036002	074	050	074	.BYTE	I!V7,I!V2,I!V7,0!V2,0!V7,0!V2	;MTK CODE 70. DATA MARK.
5383	036005	010	034	010			
5384	036010				C70	V0,V5,V0,V5,V0,V5	
5385	036010	040	064	040	.BYTE	I!V0,I!V5,I!V0,0!V5,0!V0,0!V5	;MTK CODE 70. DATA MARK.
5386	036013	024	000	024			
5387	036016				C70	V7,V2,V7,V2,V7,V2	
5388	036016	074	050	074	.BYTE	I!V7,I!V2,I!V7,0!V2,0!V7,0!V2	;MTK CODE 70. DATA MARK.
5389	036021	010	034	010			
5390	036024				C70	V0,V5,V0,V5,V0,V5	
5391	036024	040	064	040	.BYTE	I!V0,I!V5,I!V0,0!V5,0!V0,0!V5	;MTK CODE 70. DATA MARK.
5392	036027	024	000	024			
5393	036032				C70	V7,V2,V7,V2,V7,V2	
5394	036032	074	050	074	.BYTE	I!V7,I!V2,I!V7,0!V2,0!V7,0!V2	;MTK CODE 70. DATA MARK.
5395	036035	010	034	010			
5396	036040				C70	V0,V5,V0,V5,V0,V5	
5397	036040	040	064	040	.BYTE	I!V0,I!V5,I!V0,0!V5,0!V0,0!V5	;MTK CODE 70. DATA MARK.
5398	036043	024	000	024			
5399	036046				C70	V7,V2,V7,V2,V7,V2	
5400	036046	074	050	074	.BYTE	I!V7,I!V2,I!V7,0!V2,0!V7,0!V2	;MTK CODE 70. DATA MARK.
5401	036051	010	034	010			
5402	036054				C70	V0,V5,V0,V5,V0,V5	
5403	036054	040	064	040	.BYTE	I!V0,I!V5,I!V0,0!V5,0!V0,0!V5	;MTK CODE 70. DATA MARK.
5404	036057	024	000	024			

5405	036062				C70	V7, V2, V7, V2, V7, V2	
5406	036062	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5407	036065	010	034	010			
5408	036070				C70	V0, V5, V0, V5, V0, V5	
5409	036070	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5410	036073	024	000	024			
5411	036076				C70	V7, V2, V7, V2, V7, V2	
5412	036076	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5413	036101	010	034	010			
5414	036104				C70	V0, V5, V0, V5, V0, V5	
5415	036104	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5416	036107	024	000	024			
5417	036112				C70	V7, V2, V7, V2, V7, V2	
5418	036112	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5419	036115	010	034	010			
5420	036120				C70	V0, V5, V0, V5, V0, V5	
5421	036120	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5422	036123	024	000	024			
5423	036126				C70	V7, V2, V7, V2, V7, V2	
5424	036126	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5425	036131	010	034	010			
5426	036134				C70	V0, V5, V0, V5, V0, V5	
5427	036134	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5428	036137	024	000	024			
5429	036142				C70	V7, V2, V7, V2, V7, V2	
5430	036142	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5431	036145	010	034	010			
5432	036150				C70	V0, V5, V0, V5, V0, V5	
5433	036150	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5434	036153	024	000	024			
5435	036156				C70	V7, V2, V7, V2, V7, V2	
5436	036156	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5437	036161	010	034	010			
5438	036164				C70	V0, V5, V0, V5, V0, V5	
5439	036164	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5440	036167	024	000	024			
5441	036172				C70	V7, V2, V7, V2, V7, V2	
5442	036172	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5443	036175	010	034	010			
5444	036200				C70	V0, V5, V0, V5, V0, V5	
5445	036200	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, 0!V0, 0!V5	; MTK CODE 70. DATA MARK.
5446	036203	024	000	024			
5447	036206				C70	V7, V2, V7, V2, V7, V2	
5448	036206	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, 0!V7, 0!V2	; MTK CODE 70. DATA MARK.
5449	036211	010	034	010			
5450	036214				C73	V0, V5, V0, V5, V0, V5	
5451	036214	040	064	040	.BYTE	I!V0, I!V5, I!V0, 0!V5, I!V0, I!V5	; MTK CODE 73. DATA MARK.
5452	036217	024	040	064			
5453	036222				C73	V7, V2, V7, V2, V7, V2	
5454	036222	074	050	074	.BYTE	I!V7, I!V2, I!V7, 0!V2, I!V7, I!V2	; MTK CODE 73. DATA MARK.
5455	036225	010	074	050			
5456	036230						
5457	036230						
5458	036230	040	040	040			
5459	036233	000	040	040			
5460	036236						

FCKSM:

C73	V0, V0, V0, V0, V0, V0	
.BYTE	I!V0, I!V0, I!V0, 0!V0, I!V0, I!V0	; MTK CODE 73. DATA MARK.
C73	V0, V0, V0, V0, V0, V0	

MAINDEC-11-DZTCB-0  
DZTCB0.P11 18-FEB-77

TC11 TEST #2  
10:59

MACY11 27(1006) 18-FEB-77 11:33 PAGE 100  
TRAP TABLE

5461	036236	040	040	040	.BYTE	I!VO,I!VO,I!VO,O!VO,I!VO,I!VO	;MTK CODE 73. DATA MARK.
5462	036241	000	040	040			
5463	036244				C51	VO,VO,VO,VO,VO,VO	
5464	036244	040	000	040	.BYTE	I!VO,O!VO,I!VO,O!VO,O!VO,I!VO	;MTK CODE 51. FWD GUARD.
5465	036247	000	000	040			
5466	036252				C45	VO,VO,VO,VO,VO,VO	
5467	036252	040	000	000	.BYTE	I!VO,O!VO,O!VO,I!VO,O!VO,I!VO	;MTK CODE 45. REV BLOCK MARK.
5468	036255	040	000	040			
5469	036260				C25		
5470	036260	000	040	000	.BYTE	O,I,O,I,O,I	;MTK CODE 25. EXTENSION MARK.
5471	036263	040	000	040			
5472	036266				CEND		
5473	036266	377			.BYTE	-1	
5474	036267				GCKSM:		
5475	036267				C73	V7,V7,VO,VO,VO,VO	
5476	036267	074	074	040	.BYTE	I!V7,I!V7,I!VO,O!VO,I!VO,I!VO	;MTK CODE 73. DATA MARK.
5477	036272	000	040	040			
5478	036275				BCKSM:		
5479	036275				C73	VO,VO,VO,VO,VO,VO	
5480	036275	040	040	040	.BYTE	I!VO,I!VO,I!VO,O!VO,I!VO,I!VO	;MTK CODE 73. DATA MARK.
5481	036300	000	040	040			
5482	036304	036304			.EVEN		
5483	036304	000000			OPEN		
5484	036306	036306			RBUF=.		
5485	040306	040306			.RBUF+1024.		
5486	000001	000001			.END		

MAINDEC-11-DZTCB-D TC11 TEST #2  
 DZTCB0.P11 18-FEB-77 10:59

MACY11 27(1006) 18-FEB-77 11:33 PAGE 102  
 CROSS REFERENCE TABLE -- USER SYMBOLS

A	=	100000	194#		
AINCRT		015551	3207#		
APGEN0		015571	3210#		
ASETSA		015511	3201#		
A0001		002676	927	936#	
A0002		002746	941	950#	
A0003		003016	955	964#	
A0004		003066	969	978#	
A0005		003152	996	998#	
A0006		003214	1013	1015#	
A0007		003266	1027	1033#	
A0010		003340	1050#	1056	
A0011		003434	1066	1074#	
A0012		003514	1094#	1102	1105
A0013		003604	1115	1118#	
A0014		003730	1142	1144#	
A0015		004004	1158	1160#	
A0016		004056	1177	1180#	
A0017		004172	1208	1211#	
A0020		004304	1238	1241#	
A0021		004404	1257	1264#	
A0022		004476	1286	1289#	
A0023		004576	1313	1316#	
A0024		004714	1343	1349#	
A0025		005002	1371	1374#	
A0026		005076	1399	1402#	
A0027		005176	1427	1430#	
A0030		005272	1453	1456#	
A0031		005364	1479	1482#	
A0032		005626	1535	1538#	
A0033		006104	1594	1598#	
A0034		006300	1639	1642#	
A0035		006504	1687	1690#	
A0036		006710	1735	1738#	
A0037		007112	1782	1785#	
A0040		007260	1818	1821#	
A0041		007600	1890	1892#	
A0042		010056	1953	1956#	
A0043		010240	2000	2003#	
A0044		010466	2054	2057#	
A0045		010642	2094	2097#	
A0055		011372	2235	2238#	
B	=	040000	195#		
BCKSM		036275	2562	5478#	
BELL	=	000007	188#		
BIT0	=	000001	149#	227	1140 1141
BIT00	=	000001	139#	149	
BIT01	=	000002	138#	148	
BIT02	=	000004	137#	147	
BIT03	=	000010	136#	146	
BIT04	=	000020	135#	145	
BIT05	=	000040	134#	144	
BIT06	=	000100	133#	143	
BIT07	=	000200	132#	142	
BIT08	=	000400	131#	141	2645
BIT09	=	001000	130#	140	2653 2735





00041A	007670	1909	1912#	
00041B	007702	1913	1916#	
00042	010120	1945	1968#	
00043	010350	2021	2026#	
00044	010560	2063	2077#	
00045	010764	2119	2123#	
00055	011474	2237	2250#	2258#
E41	016203	494	3260#	
E410	017566	536	3417#	
E411	017742	542	3439#	
E412	020116	548	3461#	
E413	020272	554	3483#	
E414	020465	560	3508#	
E415	020632	566	3529#	
E416	021004	572	3551#	
E417	021164	578	3574#	
E42	016362	500	3283#	
E420	021344	584	3597#	
E421	021527	590	3621#	
E422	021676	596	3642#	
E423	022026	602	3661#	
E424	022201	608	3683#	
E425	022362	614	3706#	
E426	022515	620	3726#	
E427	022646	626	3746#	
E43	016523	506	3304#	
E430	023052	632	3772#	
E431	023242	638	3796#	
E432	023442	644	3822#	
E433	023610	650	3843#	
E434	023761	656	662	3865#
E435	024111	3884#		
E436	024311	666	3908#	
E437	024414	672	3923#	
E44	016727	512	3330#	
E440	024536	678	3941#	
E441	024676	684	3961#	
E442	025030	690	3980#	
E443	025170	696	4000#	
E444	025356	702	4024#	
E445	025536	708	4047#	
E446	025677	714	4068#	
E447	026052	720	4090#	
E45	017055	518	3349#	
E450	026200	726	4109#	
E451	026353	732	4132#	
E452	026535	738	4156#	
E453	026715	744	4180#	
E454	027064	750	4203#	
E455	027231	756	4225#	
E456	027416	762	4250#	
E457	027603	768	4274#	
E46	017247	524	3374#	
E460	027770	774	4299#	
E461	030161	780	4324#	
E462	030340	786	4347#	



MAINDEC-11-DZTCB-D TC11 TEST #2  
 DZTCB0.P11 18-FEB-77 10:59

MACY11 27(1006) 18-FEB-77 11:33 PAGE 106  
 CROSS REFERENCE TABLE -- USER SYMBOLS

EH63	030504	792	4368#	
EH64	030654	798	4390#	
EH65	031051	804	4416#	
EH66	031245	810	4441#	
EH67	031423	816	4464#	
EH7	017420	530	3396#	
EH70	031575	822	4486#	
EH71	031774	828	4512#	
EH72	032142	834	4534#	
EH73	032311	840	4556#	
EH74	032461	844	4577#	
EH75	032605	849	4595#	
EH76	032731	854	4613#	
EH77	033055	859	4631#	
ENTVEC=	000030	159#	879#	880*
ENTX =	000000	228#		
EH1	016115	493	3250#	
EH10	017514	535	3410#	
EH11	017662	541	3431#	
EH12	020036	547	3453#	
EH13	020212	553	3475#	
EH14	020366	559	3497#	
EH15	020562	565	3522#	
EH16	020726	571	3543#	
EH17	021100	577	3565#	
EH2	016300	499	3274#	
EH20	021260	583	3588#	
EH21	021440	589	3611#	
EH22	021624	595	3635#	
EH23	021772	601	3656#	
EH24	022122	607	3675#	
EH25	022276	613	3697#	
EH26	022456	619	3720#	
EH27	022604	625	3740#	
EH3	016456	505	3297#	
EH30	022742	631	3760#	
EH31	023146	637	3786#	
EH32	023364	643	3814#	
EH33	023536	649	3836#	
EH34	023704	655	661	3857#
EH35	024056	3879#		
EH36	024234	665	3900#	
EH37	024406	671	3922#	
EH4	015620	511	3318#	
EH40	024510	677	3937#	
EH41	024632	683	3955#	
EH42	024772	689	3975#	
EH43	025124	695	3994#	
EH44	025314	701	4018#	
EH45	025502	707	4042#	
EH46	025662	713	4065#	
EH47	025774	719	4082#	
EH5	017024	517	3344#	
EH50	026146	725	4104#	
EH51	026310	731	4126#	
EH52	026476	737	4150#	

EM53	026644	743	4173#
EM54	027024	749	4197#
EM55	027172	755	4219#
EM56	027340	761	4242#
EM57	027524	767	4266#
EM6	017152	523	3363#
EM60	027712	773	4291#
EM61	030076	779	4315#
EM62	030302	785	4342#
EM63	030446	791	4363#
EM64	030626	797	4386#
EM65	030762	803	4406#
EM66	031146	809	4430#
EM67	031342	815	4455#
EM7	017344	529	3388#
EM70	031520	821	4478#
EM71	031726	827	4505#
EM72	032102	833	4528#
EM73	032250	839	4550#
EM74	032406	843	4569#
EM75	032532	848	4587#
EM76	032656	853	4605#
EM77	033002	858	4623#
ERRVEC=	000004	152#	895
ET1	016262	495	3269#
ET10	017644	537	3426#
ET11	020020	543	3448#
ET12	020174	549	3470#
ET13	020350	555	3492#
ET14	020544	561	3517#
ET15	020710	567	3538#
ET16	021062	573	3560#
ET17	021242	579	3583#
ET2	016440	501	3292#
ET20	021422	585	3606#
ET21	021606	591	3630#
ET22	021754	597	3651#
ET23	022104	603	3670#
ET24	022260	609	3692#
ET25	022440	615	3715#
ET26	022570	621	3735#
ET27	022724	627	3755#
ET3	016602	507	3313#
ET30	023130	633	3781#
ET31	023342	639	3808#
ET32	023520	645	3831#
ET33	023666	651	3852#
ET34	024040	657	663
ET35	024214	3897#	
ET36	024370	667	3917#
ET37	024472	673	3932#
ET4	017006	513	3339#
ET40	024614	679	3950#
ET41	024754	685	3970#
ET42	025106	691	3989#
ET43	025272	697	4012#

896\* 907\* 2636 2637\* 2639\* 2642\*

3874#



























	2223	2265	2277																
SETPRI	164#																		
SETRAP	259#																		
SETTRA	3119#	3145	3158	3163	3168	3173													
SETUP	164#	868																	
SKIP	164#																		
SLASH	164#																		
SPACE	164#																		
STARS	14#	164#	343	444	2269	2608	2691	2751	2783	2820	2892	2968	3047	3097					
SWRSU	164#	891#	892																
TRMTRP	3141#																		
TYPBIN	164#																		
TYPDEC	164#	2290																	
TYPNAM	164#																		
TYPNUM	164#																		
TYPPCS	164#																		
TYP OCT	164#	3060	3085																
TYPTXT	164#																		
SSCHRE	327#	386	389	392	395	398	401	404	407										
SSCHTM	334#	414	417	420	423	426	429	432	435										
SSESCA	164#																		
SSNEWT	164#																		
SSSET	3125#	3146	3159	3164	3169	3174													
SSSKIP	164#																		
.EQUAT	11#	53																	
.HEADE	11#	18																	
.SETUP	12#	16	862																
.SWRHI	12#	29																	
.SWRLO	12#	42#																	
.SCATC	11#	166																	
.SCHTA	15#	326																	
.SEOP	11#	2266																	
.SERRO	14#	2688																	
.SERRT	14#	3044																	
.SPOWE	13#	2748																	
.SSCOP	12#	2605																	
.STRAP	13#	3094																	
.STYPD	13#	2889																	
.STYPE	14#	2817																	
.STYPO	13#	2965																	

. ABS. 040306 000

ERRORS DETECTED: 0  
DEFAULT GLOBALS GENERATED: 0

DZTCB0.BIN DZTCB0.LST/CRF/SOL=DZTCB0.P11  
RUN-TIME: 19 12 2 SECONDS  
RUN-TIME RATIO: 157/35=4.4  
CORE USED: 22K (44 PAGES)